ANALOG ELECTRONIC CIRCUITS

Lecture Notes

B.TECH

Academic Session: (2023-24)

Department of Electrical Engineering

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SYNERGY
A Modern Day Gurukul

SYNERGY INSTITUTE OF ENGINEERING & TECHNOLOGY

Name of the Faculty: Bishnupriya Sahoo

Course : B.TECH

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Semester : 3RD

Name of the subject : ANALOG ELECTRONIC CIRCUITS

Subject Code : REE3C001

Subject Credit : 03

Syllabus

MODULE – I **(12 Hours)**

MOS Field-Effect Transistor: Principle and Operation of FETs and MOSFETs; P-Channel and N-Channel MOSFET; Complimentary MOS; V-I Characteristics of E- MOSFET and D-MOSFET; MOSFET as an Amplifier and as a Switch.
Biasing of BJTs: Load lines (AC and DC); Operating Points; Fixed Bias and Self Bias, DC Bias with Voltage Feedback; Bias Stabilization; Examples.
Biasing of FETs and MOSFETs: Fixed Bias Configuration and Self Bias Configuration, Voltage Divider Bias and Design

MODULE – II **(12 Hours)**

Small Signal Analysis of BJTs: Small-Signal Equivalent-Circuit Models; Small Signal Analysis of CE, CC, CB amplifiers. Effects of R_S and R_L on CE amplifier operation, Emitter Follower; Cascade amplifier, Darlington Connection and Current Mirror Circuits.
Small Signal Analysis of FETs: Small-Signal Equivalent-Circuit Model, Small Signal Analysis of CS, CD, CG Amplifiers. Effects of R_{SIG} and R_L on CS Amplifier; Source Follower and Cascaded System.

MODULE – III **(8 hours)**

High Frequency Response of FETs and BJTs: High Frequency equivalent models and frequency Response of BJTs and FETs; Frequency Response of CS Amplifier, Frequency Response of CE Amplifier.

MODULE – IV **(6 hours)**

Feedback amplifier and Oscillators: Concepts of negative and positive feedback; Four Basic Feedback Topologies, Practical Feedback Circuits, Principle of Sinusoidal Oscillator, Wein-Bridge, Phase Shift and Crystal Oscillator Circuits, Power Amplifier (Class A, B, AB, C).

MODULE – V **(7 hours)**

Operational Amplifier: Ideal Op-Amp, Differential Amplifier, Op-Amp Parameters, Non-inverting Configurations, Open-loop and Closed-loop Gains, Differentiator and Integrator, Instrumentation amplifier.

Books:

- *Microelectronics Circuits, Adel Sedra and Kenneth C Smith, Oxford University Press, New Delhi, 5th Edition, International Student Edition,2009. (Selected portion of Chapter 2,4, 5, 6, 8, 13, and 14)*
- *Electronic Devices and Circuits theory, R.L. Boylestad and L. Nashelsky, Pearson Education, New Delhi , 9th/10th Edition,2013. (Selected portions of Chapter 4, 5, 6, 7, 8, 9, 10, 11, 12, and 14)*
- *Milliman's Electronics Devices and Circuits, J. Milliman, C. Halkias, S. Jit., Tata McGraw Hill Education Pvt. Ltd., New Delhi, 2nd Edition,2008.*
- *Electronic Devices and Circuits, Jimmie J. Cathey adapted by Ajay Kumar Singh, Tata McGraw Hill Publishing Company Ltd., New Delhi, 3rd Edition, (For Problem Solving)*

Biasing of BJTs

Bipolar Junction Transistor

Introduction

The transistor is a solid state device, whose operation depends upon the flow of electric charge carriers within the solid. Transistor is capable of amplification and in most respect it is analogous to a vacuum triode. The main difference between two is that the transistor is a current controlled device whereas vacuum triode is a voltage controlled device. The transistor is only about 6 decade old, yet it is replacing vacuum triode in almost all applications. The reasons are obviously its advantages over vacuum tubes such as

- ✓ Compact size
- ✓ Light weight
- ✓ Rugged construction
- ✓ More resistive to shocks and vibrations
- ✓ Instantaneous operation (no heating required)
- ✓ Low operating voltage
- ✓ High operating efficiency (no heat loss)
- ✓ Long life

However, transistors, in comparison to vacuum triodes, have some drawbacks also such as loud hum noise, restricted operating temperature (up to 75^0C) and operating frequency (up to a few MHz only).

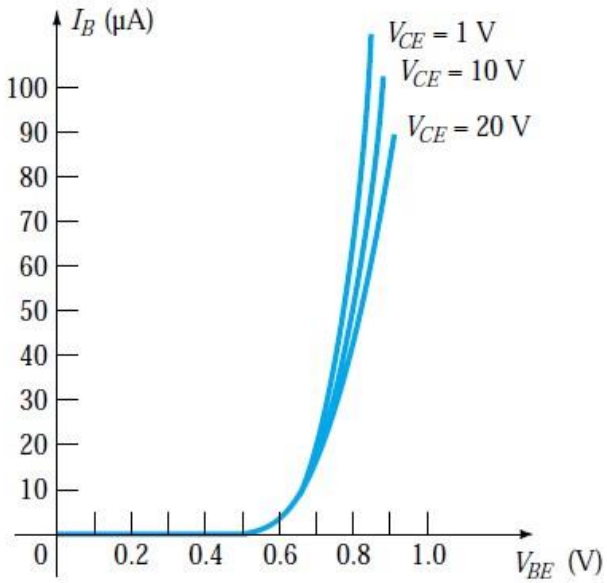
Characteristics of CE transistor

Input characteristics

- ✓ The curve drawn between base current I_B and base-emitter voltage V_{BE} for a given value of collector-emitter voltage V_{CE} is known as the input characteristics.

- ✓ For determination of input characteristics, collector-emitter voltage $V_{CE}$is held constant and base current $I_B$is recorded for different values of base-emitter voltageV_{BE}.

- ✓ Now the curves are drawn between base current I_B and base-emitter voltage V_{BE} for different values of V_{CE}, as shown in figure



- ✓ The input characteristics of CE transistors are quiet similar to those of a forward biased diode because the bas-emitter region of the transistor is a diode and it is forward biased.

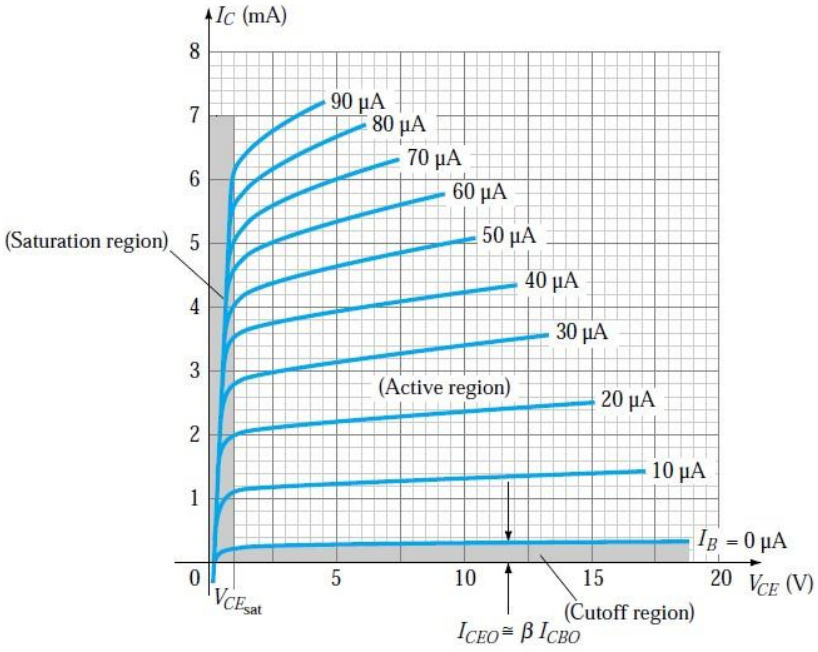
Output Characteristics

- ✓ Output characteristic of a common emitter transistor is the curve drawn between collector current I_C and collector-emitter voltage $V_{CE}$for a given value of base currentI_B.

- ✓ For determination of common emitter output characteristics, base current I_B is maintained at several convenient levels.

- ✓ At each fixed level of I_B, collector-emitter voltage V_{CE} is adjusted in steps, and the corresponding values of collector current I_C are noted.

- ✓ Thus, a family of characteristics is obtained which are typically as illustrated in Figure



The points regarding output characteristics are given below

- ✓ The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V and then becomes almost constant and independent ofV_{CE}. The transistors are always operated above 1V.

- ✓ Output characteristic in CE configuration has some slope while CB configuration has almost horizontal characteristics.

- ✓ In active region (collector junction reverse biased and emitter junction forward biased), for small values of base current $I_B$the effect of collector voltage over I_C is small but for large values of $I_C$this effect increases.

- ✓ With low values (ideally zero) of $V_{CE}$the transistor is said to be operated in saturation region and in this region base current I_B does not cause a corresponding change in collector currentI_C.

- ✓ With much higher V_{CE}, the collector-base junction completely breakdown and because of this avalanche breakdown collector current I_C increases rapidly and the transistor gets damaged.

- ✓ In cut off region, small amount of collector current I_C flows even when base current $I_B = 0$. This is called I_{CEO}. Since main current I_C is zero, the transistor is said to be cut-off.

Faithful Amplification

The basic function of transistor is to do amplification.

The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. This increase in magnitude of the signal without any change in shape is known as *faithful amplification*.

In order to achieve this, means are provided to ensure that input circuit (*i.e.* baseemitter junction) of the transistor remains forward biased and output circuit (*i.e.* collector base junction) always remains reverse biased during all parts of the signal. This is known as *transistor biasing*.

The process of raising the strength of a weak signal without any change in its general shape is known as faithful amplification.

The theory of transistor reveals that it will function properly if its input circuit (i.e. base-emitter junction) remains forward biased and output circuit (i.e. collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied.

(i) Proper zero signal collector current

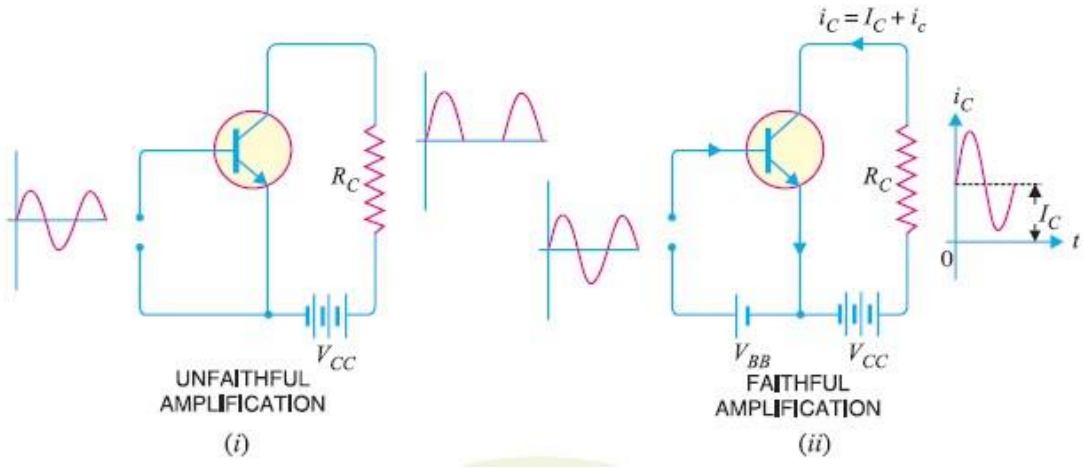
(ii) Minimum proper base-emitter voltage (V_{BE}) at any instant

(iii) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (i) and (ii) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (iii) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics i.e. between saturation to cut off.

Proper zero signal collector current

Consider an npn transistor circuit shown in Fig. During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.



Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as zero signal collector current I_C. During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal

collector current must flow. The value of zero signal collector current should be at least equal to the maximum collector current due to signal alone i.e.

Zero signal collector current Maximum collector current due to signal alone

Proper minimum base-emitter voltage.

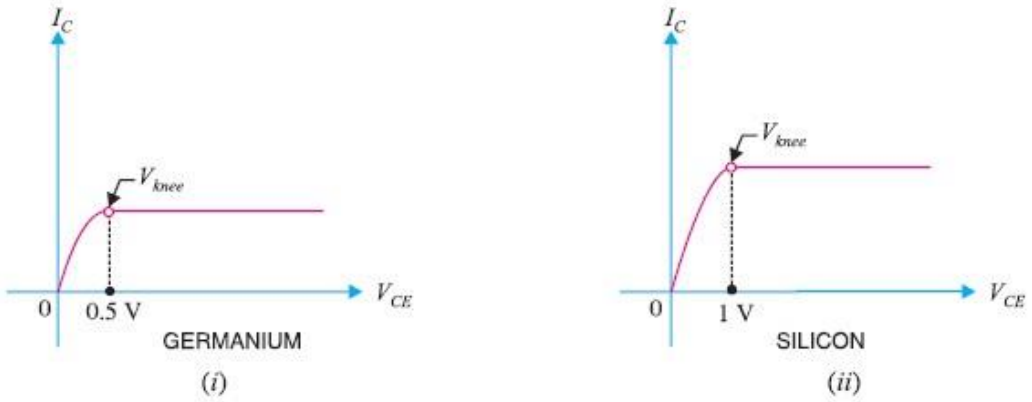
In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for Si transistors at any instant.

The base current is very small until the input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for Si transistors as shown in Fig. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current.

This will result in unfaithful amplification.

Proper minimum V_{CE} at any instant.

For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called knee voltage (See Fig.).

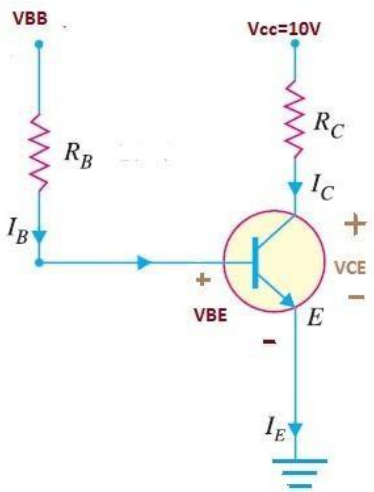


When V_{CE} is too low (less than 0.5V for Ge transistors and 1V for Si transistors), the collector base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if V_{CE} is allowed to fall below V_{Knee} during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when V_{CE} is greater than V_{Knee}, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

Numerical:

For the circuit shown in the Fig. has $R_B = 10\ K\Omega$ and$R_C = 1\ K\Omega$, it is required to determine the value of V_{BB} that results the transistor operating a) in the active mode with $V_{CE} = 5V$, b) at the edge of saturation c) deep in saturation with $\beta_{forced} = 10$

For simplicity, assume that$V_{BE} = 0.7V$. The transistor has $\beta = 50$



a) $$I_C = \frac{V_{CC}-V_{CE}}{R_C} = \frac{10V-5V}{1K\Omega} = 5mA$$

$$I_B = {I_C}/{\beta} = \frac{5mA}{50} = 0.1mA$$

$$V_{BB} = I_B R_B + V_{BE}$$

$$= 0.1 \times 10 + 0.7 = 1.7V$$

b) $$\boldsymbol{V_{CE} = V_{CEsat} \approx 0.3V}$$

$$I_C = \frac{V_{CC}-V_{CE_{sat}}}{R_C} = \frac{10V-0.3V}{1K\Omega} = 9.7mA$$

$$I_B = {I_C}/{\beta} = \frac{9.7mA}{50} = 0.194mA$$

$$V_{BB} = I_B R_B + V_{BE}$$

$$= 0.194 \times 10 + 0.7 = 2.64V$$

c) $$\boldsymbol{V_{CE} = V_{CEsat} \approx 0.2V}$$

$$I_C = \frac{V_{CC} - V_{CE_{sat}}}{R_C} = \frac{10V - 0.2V}{1K\Omega} = 9.8mA$$

$$I_B = {I_C}/{\beta_{forced}} = \frac{9.8mA}{10} = 0.98mA$$

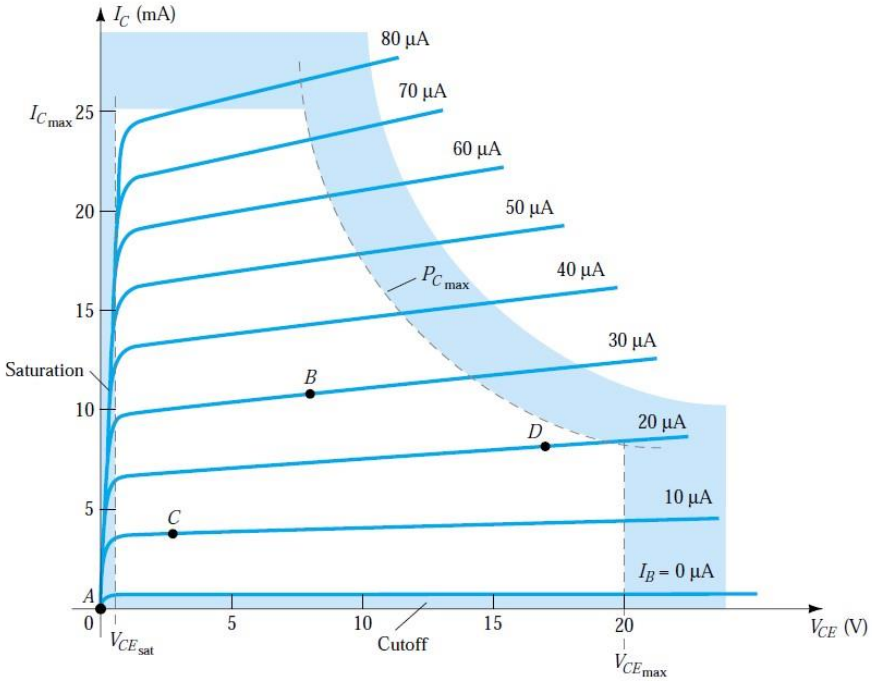
$$V_{BB} = I_B R_B + V_{BE}$$

$$= 0.98 \times 10 + 0.7 = 10.5V$$

OPERATING POINT

For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the

applied signal. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point). By definition, quiescent means quiet, still, inactive. Figure shows a general output device characteristic with four operating points indicated.



Point A

If no bias were used, the device would initially be completely off, resulting in a *Q*point at *A*-namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal therefore point *A* would not be suitable.

Point C

At point C near cut-off region, the output current I_C and output voltage V_{CE} would be allowed to vary, but clipped at negative peaks for a sinusoidally varying signal. So it is not the suitable operating point.

Point B

In this case when the signal is applied to the circuit, collector voltage and current will vary approximately symmetrical around the quiescent values of I_C and V_{CE} and amplify both positive and negative parts of input signal. In this case the voltage and current of the device will vary, but not enough to drive the device into saturation or cut off region. Usually, the amplifier action occurs within the operating region of the device between cut-off and saturation. So at point B located at centre of the load line is the best operating point in terms of linear gain or largest possible voltage and current swing variation.

Bias Stabilisation

The collector current in a transistor changes rapidly when

- ✓ The temperature changes,
- ✓ The transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (*i.e*. zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates to make the operating point independent of these variations. This is known as bias stabilisation.

The process of making operating point independent of temperature changes or variations in transistor parameters is known as bias **stabilisation.**

Once stabilisation is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor *i.e*. the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation

Stabilisation of the operating point is necessary due to the following reasons:

- ✓ Temperature dependence of I_C
- ✓ Individual variations
- ✓ Thermal runaway

Temperature dependence of I_C

The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

The collector leakage current I_{CO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point *i.e*. to hold I_C constant inspite of temperature variations.

Individual variations

The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilise the operating point i.e. to hold I_C constant irrespective of individual variations in transistor parameters.

Thermal runaway.

The collector current for a CE configuration is given by :

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

The collector leakage current I_{CO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CO} also increases. It is clear from exp. (i) that if I_{CO} increases, the collector current I_C increases by $(\beta + 1)\ I_{CO}$. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out.

The self-destruction of an unstabilised transistor is known as **thermal runaway.**

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised i.e. I_C is kept constant. In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in $\beta\ I_B$ will compensate for the increase in $(\beta + 1)\ I_{CO}$, keeping Ic nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

Stability Factor

Stability Factor due to leakage current

It is desirable and necessary to keep I_C constant in the face of variations of I_{CO}. The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor S. It is defined as under:

The rate of change of collector current I_C w.r.t. the collector leakage current I_{CO} at constant β and V_{BE} is called stability factor i.e.

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad \text{Where } V_{BE} \text{ and } \beta \text{ are constant}$$

The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}. Thus stability factor 50 of a circuit means that I_C changes 50 times as much as any change in I_{CO}. In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible. The ideal value of S is 1 but it is never possible to achieve it in practice. Experience shows that values of S exceeding 25 result in unsatisfactory performance.

Stability Factor due to base-emitter voltage V_{BE}

The rate of change of collector current I_C w.r.t. base-emitter voltage at constant β and I_{CO} is called stability factor due to base-emitter voltage i.e.

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \quad \text{Where } \beta \text{ and } I_{CO} \text{ are constant}$$

Stability Factor due to β

The rate of change of collector current I_C w.r.t. β at constant base-emitter voltage and I_{CO} is called stability factor due to current gain β i.e.

$$S(\beta) = \frac{dI_C}{d\beta} \quad \text{Where } V_{BE} \text{ and } I_{CO} \text{ are constant}$$

General expression for $S(I_{CO})$

In the active region, the basic relationship between I_C and I_B is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

Differentiating both sides w.r.t I_C keeping β as constant

$$\frac{dI_C}{dI_C} = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

$$1 - \beta \frac{dI_B}{dI_C} = (\beta + 1) \frac{1}{S(I_{CO})}$$

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

The value of $\frac{dI_B}{dI_C}$ depends upon the biasing arrangement used and for determination of the stability factor S (I_{CO}) it is only necessary to find the relationship between I_C and I_B.

General expression for S (β)

In the active region, the basic relationship between I_C and I_B is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

Differentiating both sides w.r.t I_C keeping I_{CO} as constant

$$1 = \beta \frac{dI_B}{dI_C} + I_B \frac{d\beta}{dI_C} + I_{CO} \frac{d\beta}{dI_C}$$

$$\frac{d\beta}{dI_C}(I_B + I_{CO}) = 1 - \beta \frac{dI_B}{dI_C}$$

$$\frac{1}{S(\beta)}(I_B + I_{CO}) = 1 - \beta\frac{dI_B}{dI_C}$$

$$S(\beta) = \frac{I_{CO} + I_B}{1 - \beta\frac{dI_B}{dI_C}}$$

Transistor Biasing

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely: (i) proper zero signal collector current, (ii) proper base-emitter voltage at any instant and (iii) proper collector-emitter voltage at any instant. It is the fulfilment of these conditions which is known as transistor biasing.

The proper flow of zero signal collector current and the maintenance of proper collectoremitter voltage during the passage of signal is known as *transistor biasing*.

The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as biasing circuit. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

Methods of Transistor Biasing

In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery V_{BB} which was separate from battery V_{CC} used in the output circuit. However, in the interest of simplicity and economy it is desirable that transistor circuit should have a single source of supply—the one in the output circuit i.e V_{CC}). The following are the most commonly used methods of obtaining transistor biasing from one source of supply V_{CC}.

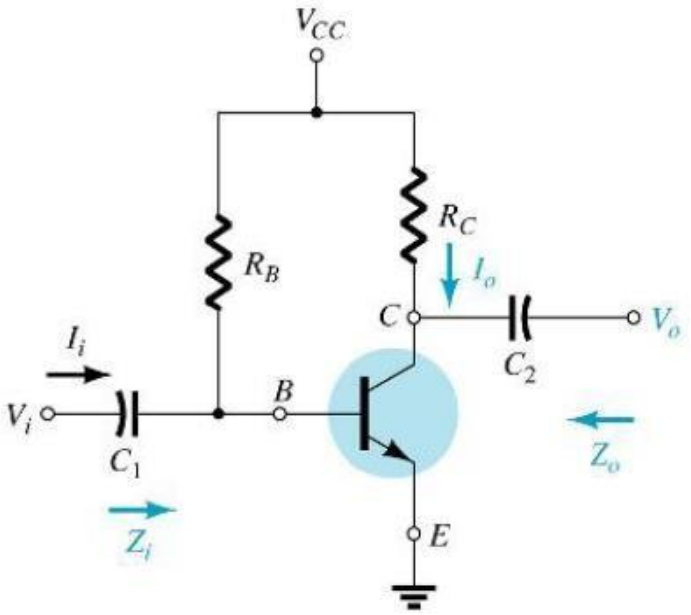
- ✓ Base resistor or fixed bias method

- ✓ Emitter bias method
- ✓ Biasing with collector-feedback resistor
- ✓ Voltage-divider bias

In all these methods, the same basic principle is employed i.e. required value of base current (and hence I_C) is obtained from V_{CC} in the zero signal conditions. The value of collector load R_C is elected keeping in view that V_{CE} should not fall below 0.5 V for germanium transistors and 1V for silicon transistor.

Fixed-Bias Circuit

In this method, a high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply for *npn* transistor (See Fig.) and between base and negative end of supply for *pnp* transistor. Here, the required zero signal base current is provided by V_{CC} and it flows through R_B. It is because now base is positive *w.r.t.* emitter *i.e.* base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.



Input loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since V_{BE} is small as compared to V_{CC}

$$I_B \cong \frac{V_{CC}}{R_B}$$

Output loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

Stability Factors in Fixed-bias Circuit

S (I_{CO}):-

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad Where\ V_{BE}\ and\ \beta\ are\ constant$$

General expression for S (I_{CO}) is given by

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

Since in fixed-biasing method I_B is independent of I_C

i.e.

$$\frac{dI_B}{dI_C} = 0$$

$$\boxed{S\,(I_{CO}) = \beta + 1}$$

If β=150 S (I_{CO}) =151 which means that collector current I_C increases 151 times as much as I_{CO}. Such a large value of S (I_{CO}) makes thermal runaway, a definite possibility with this circuit.

S (V_{BE}):-

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \quad Where\ \beta\ and\ I_{CO}\ are\ constant$$

In fixed-bias circuit the input loop equation is given by

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Differentiating w.r.t. I_C keeping β constant, we get

$$\frac{dV_{CC}}{dI_C} - \frac{1}{\beta} R_B - \frac{dV_{BE}}{dI_C} = 0$$

$$\boxed{S(V_{BE}) = \frac{-\beta}{R_B}}$$

S (β):-

$$S(\beta) = \frac{dI_C}{d\beta} \quad Where\ V_{BE}\ and\ I_{CO}\ are\ constant$$

General expression for S (β) is given by

$$S(\beta) = \frac{I_{CO} + I_B}{1 - \beta \frac{dI_B}{dI_C}}$$

Since in fixed- biasing method I_B is independent of I_C i.e.

$$\frac{dI_B}{dI_C} = 0$$

$$S(\beta) = I_{CO} + I_B$$

Advantages:

- ✓ This biasing circuit is very simple as only one resistance R_B is required.
- ✓ Biasing conditions can easily be set and the calculations are simple.
- ✓ There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages:

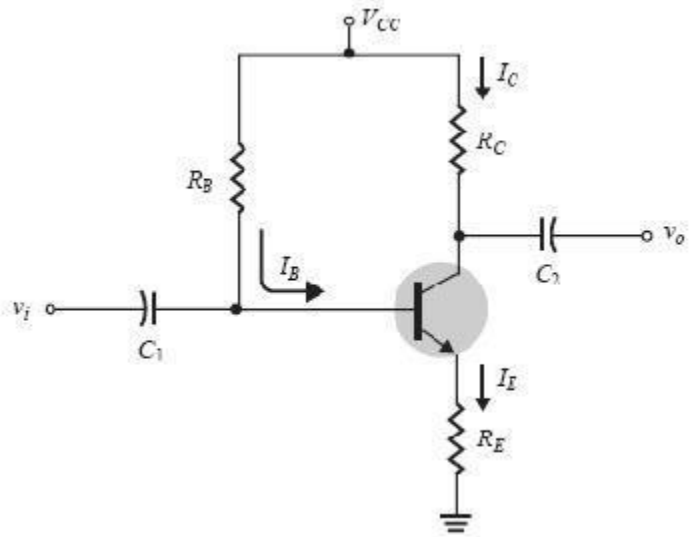
- ✓ This method provides poor stabilisation. It is because there is no means to stop a self increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.

- ✓ The stability factor is very high. Therefore, there are strong chances of thermal runaway.

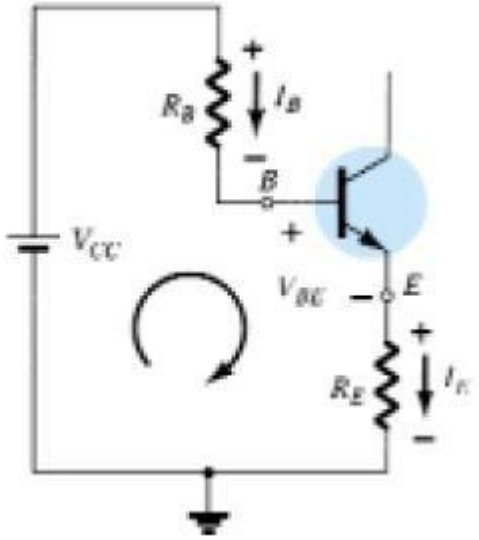
Due to these disadvantages, this method of biasing is rarely employed.

Emitter-Stabilised Bias Circuit

It can be shown that, including an emitter resistor in the fixed bias circuit improves the stability of Q point. Thus emitter bias is a biasing circuit very similar to fixed bias circuit with an emitter resistor added to it.



Input Loop



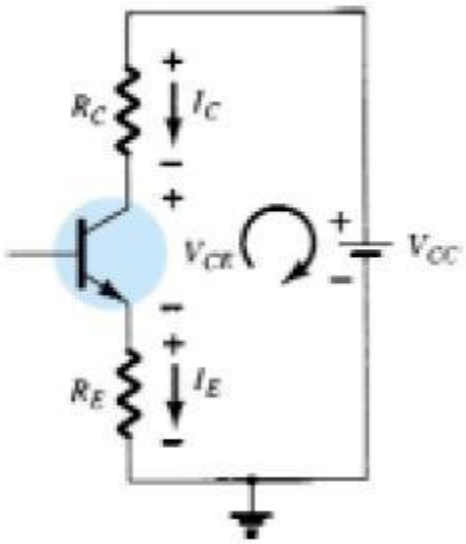
Writing KVL around the input loop we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

Output loop



Collector – emitter loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

I_C is almost same as I_E

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

Stability Factors in Emitter-Stabilized bias Circuit

S (I_{CO}):-

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad Where\ V_{BE}\ and\ \beta\ are\ constant$$

From the input circuit we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C)\, R_E = 0$$

Differentiating above w.r.t. I_C keeping V_{BE} as constant

$$\frac{dV_{CC}}{dI_C} - R_B \frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} - R_E \frac{dI_B}{dI_C} - R_E = 0$$

$$-(R_B + R_E)\frac{dI_B}{dI_C} - R_E = 0$$

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

General expression for S (I_{CO}) is given by

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

So, the Stability Factor due to leakage current in Emitter-Stabilized bias Circuit is

$$\boxed{S(I_{CO}) = \frac{\beta + 1}{1 + \beta \frac{R_E}{R_E + R_B}}}$$

S (V_{BE}):-

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \qquad Where\ \beta\ and\ I_{CO}\ are\ constant$$

In self-bias circuit the input loop equation is given by

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - \frac{I_C}{\beta} R_B - V_{BE} - (\beta + 1)\frac{I_C}{\beta} R_E = 0$$

Differentiating above w.r.t. I_C keeping β as constant

$$\frac{dV_{CC}}{dI_C} - \frac{R_B}{\beta} - \frac{dV_{BE}}{dI_C} - \frac{\beta + 1}{\beta} R_E = 0$$

$$-\left[\frac{R_B}{\beta} + \frac{(\beta + 1)}{\beta} R_E\right] = \frac{dV_{BE}}{dI_C}$$

So, the Stability Factor due to base emitter voltage in Emitter-Stabilized bias Circuit is

$$S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E}$$

S (β):-

$$S(\beta) = \frac{dI_C}{d\beta} \quad Where\ V_{BE}\ and\ I_{CO}\ are\ constant$$

General expression for S (β) is given by

$$S(\beta) = \frac{I_{CO} + I_B}{1 - \beta \frac{dI_B}{dI_C}}$$

In self-bias circuit

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

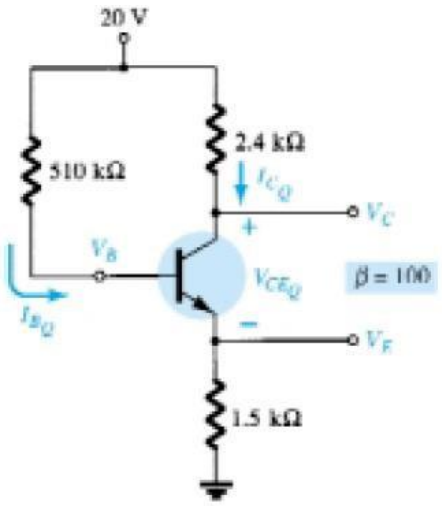
So, the Stability Factor due to current gain β in Emitter-Stabilized bias Circuit is

$$\boxed{S(\beta) = \frac{I_{CO} + I_B}{1 + \beta \frac{R_E}{R_E + R_B}}}$$

Numerical

For the network shown in Fig. determine the following

a) I_{BQ} b) I_{CQ}c) V_{CEQ}d) V_C e) V_B



Solution:

a) Applying KVL at the input circuit

$$20 - (510K)I_B - 101 \times I_B \times (1.5K) = 0$$

$$I_{BQ} = 29.17\mu A$$

b) $I_{CQ} = \beta I_{BQ} = 2.91mA$

c) $I_E = (\beta + 1)I_B = 101 \times (29.17\mu A) = 2.94mA$

$$20 - 2.91 \times 2.4 - V_{CE} - 2.94 \times 1.5 = 0$$

$$V_{CEQ} = 8.59V$$

d) $20 - 2.91 \times 2.4 - V_C = 0$

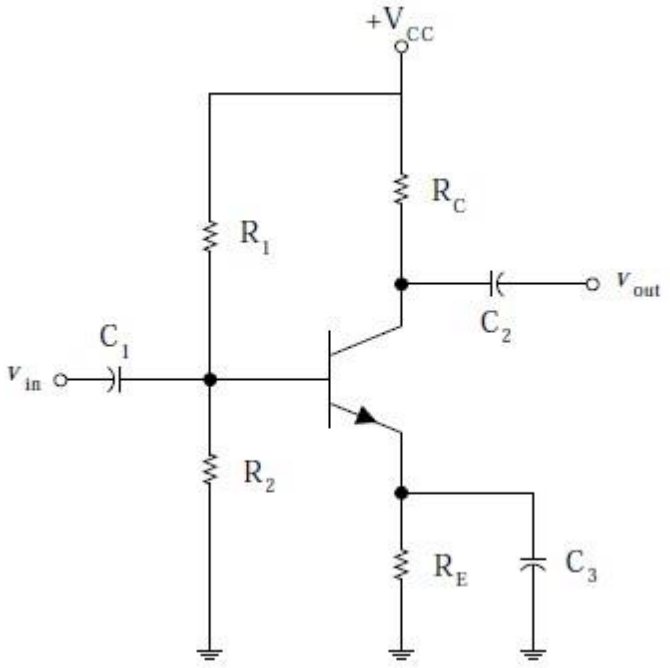
$$V_C = 13V$$

e) $V_E = I_E R_E = 2.94 \times 1.5 = 4.41V$

$$V_{BE} = V_B - V_E$$

$$V_B = V_{BE} + V_E = 0.7 + 4.41 = 5.11V$$

Voltage-divider Bias Circuit



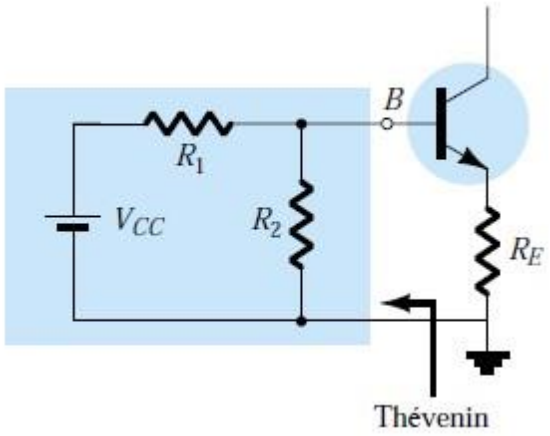
- ✓ This is the biasing circuit wherein, I_{CQ} and V_{CEQ} are almost independent of β.
- ✓ The level of I_{BQ} will change with β so as to maintain the values of I_{CQ} and V_{CEQ} almost same, thus maintaining the stability of Q point.

Two methods of analysing a voltage divider bias circuit are:

- ✓ **Exact method** – can be applied to any voltage divider circuit
- ✓ **Approximate method** – direct method, saves time and energy, can be applied in most of the circuits.

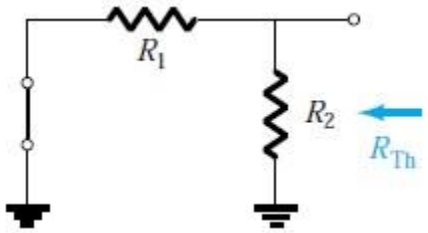
Exact method

In this method, the Thevenin equivalent network for the network to the left of the base terminal to be found.



To find R_{th}:

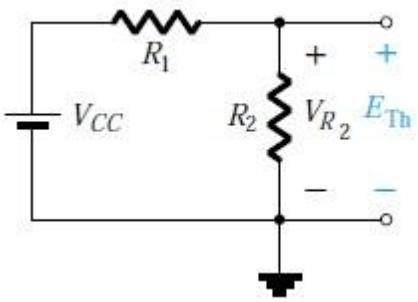
The voltage source is replaced by short-circuit equivalent as shown in figure



$R_{th} = R_1 \| R_2$

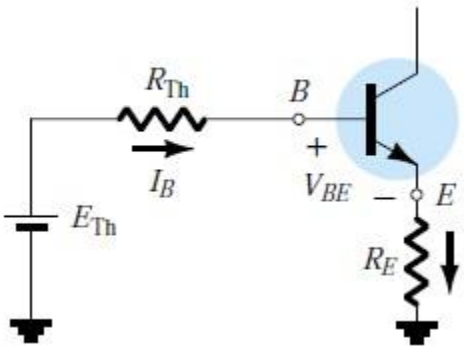
To find E_{th}:

The voltage source $V_{CC}$is returned to the network and the open-circuit Thevenin voltage of Fig. determined as follows:



$$E_{th} = \frac{V_{CC}R_2}{R_1 + R_2}$$

The Thevenin network is then redrawn as shown in Fig, and $I_B$can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:



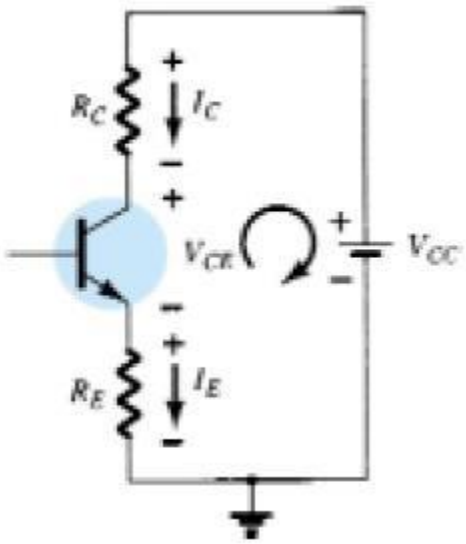
Applying KVL in the base-emitter loop

$$E_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$E_{th} - I_B R_{th} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$I_B = \frac{E_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$

Output loop



Collector – emitter loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

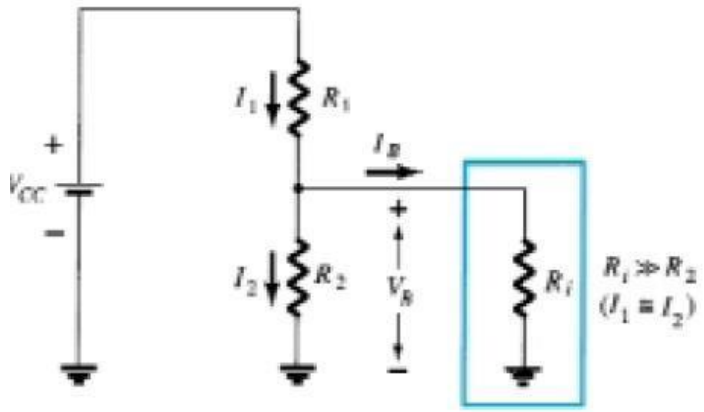
I_C is almost same as I_E

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Approximate method

The input section of the voltage-divider configuration can be represented by the network of Fig. The resistanceR_i is the equivalent resistance between base and ground for the transistor with an emitter resistorR_E. The reflected resistance between base +and emitter is defined by$R_i = (\beta + 1)R_E$. If R_i is much larger than the resistanceR_2, the current $I_B$will be much smaller than I_2 (current

always seeks the path of least resistance) and I_2 will be approximately equal toI_1. If we accept the approximation that $I_B$is essentially zero amperes compared to I_1orI_2, then $I_1 = I_2$and $R_1$and R_2can be considered series elements.



The voltage acrossR_2, which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Since $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition that will define whether the approximate approach can be applied will be the following:

$$\beta R_E \geq 10R_2$$

In other words, if β times the value ofR_E is at least 10 times the value ofR_2, the approximate approach can be applied with a high degree of accuracy.

Once $V_B$is determined, the level of $V_E$can be calculated from

$$V_E = V_B - V_{BE}$$

And the emitter current can be determined from

$$I_E = \frac{V_E}{R_E}$$

$$I_{CQ} \cong I_E$$

The collector-to-emitter voltage is given by,

$$V_{CE} = V_{CC} - I_C R_C$$

Stability Factors in Voltage-divider bias Circuit

S (I_{CO}):-

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad Where\ V_{BE}\ and\ \beta\ are\ constant$$

From the input circuit we get

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_{Th} - V_{BE} - (I_B + I_C)\, R_E = 0$$

Differentiating above w.r.t. I_C keeping V_{BE} as constant

$$\frac{dV_{Th}}{dI_C} - R_{Th}\frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} - R_E\frac{dI_B}{dI_C} - R_E = 0$$

$$-(R_{Th}+R_E)\frac{dI_B}{dI_C}-R_E=0$$

$$\frac{dI_B}{dI_C}=\frac{-R_E}{R_{Th}+R_E}$$

General expression for S (I_{CO}) is given by

$$S(I_{CO})=\frac{\beta+1}{1-\beta\frac{dI_B}{dI_C}}$$

So, the Stability Factor due to leakage current in Voltage-divider bias Circuit is

$$\boxed{S(I_{CO})=\frac{1+\beta}{1+\beta\frac{R_E}{R_E+R_{Th}}}}$$

S (V_{BE}):-

$$S(V_{BE})=\frac{dI_C}{dV_{BE}} \quad Where\ \beta\ and\ I_{CO}\ are\ constant$$

In Voltage-divider bias circuit the input loop equation is given by

$$V_{Th}-I_BR_{Th}-V_{BE}-I_ER_E=0$$

$$V_{Th}-\frac{I_C}{\beta}R_{Th}-V_{BE}-(\beta+1)\frac{I_C}{\beta}R_E=0$$

Differentiating above w.r.t. I_C keeping β as constant

$$\frac{dV_{Th}}{dI_C}-\frac{R_{Th}}{\beta}-\frac{dV_{BE}}{dI_C}-\frac{\beta+1}{\beta}R_E=0$$

$$-\left[\frac{R_{Th}}{\beta}+\frac{(\beta+1)}{\beta}R_E\right]=\frac{dV_{BE}}{dI_C}$$

So, the Stability Factor due to base emitter voltage in Voltage-divider bias Circuit is

$$S(V_{BE})=\frac{-\beta}{R_{Th}+(\beta+1)R_E}$$

S (β):-

$$S(\beta)=\frac{dI_C}{d\beta} \quad Where\ V_{BE}\ and\ I_{CO}\ are\ constant$$

General expression for S (β) is given by

$$S(\beta)=\frac{I_{CO}+I_B}{1-\beta\frac{dI_B}{dI_C}}$$

In voltage-divider circuit

$$\frac{dI_B}{dI_C}=\frac{-R_E}{R_{Th}+R_E}$$

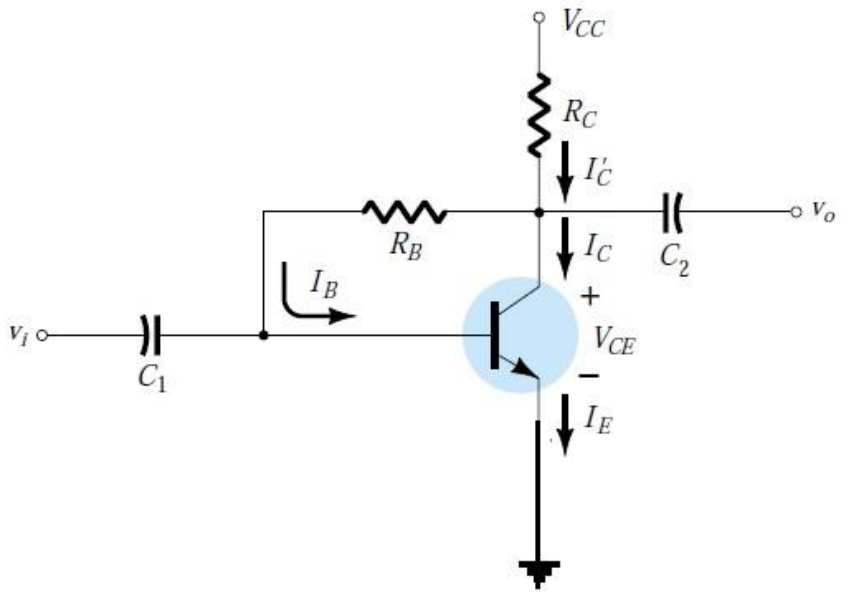
So, the Stability Factor due to current gain β in Voltage-divider bias Circuit is

$$S(\beta)=\frac{I_{CO}+I_B}{1+\beta\frac{R_E}{R_E+R_{Th}}}$$

Collector-to-Base Bias

(Or Base-bias with Collector Feedback)

This circuit is like a fixed bias circuit except that base resistor R_B is returned to the collector terminal instead ofV_{CC}. It derives its name from the fact that voltage for R_B is derived from collector. There exists a negative feedback effect which tends to stabilize $I_C$against changes either as a result of change in temperature or as a result of replacement of the transistor by another one.

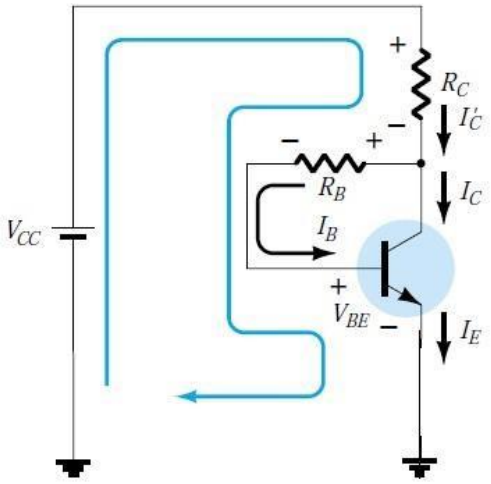


Circuit Operation

If the collector current I_C tends to increase (either due to rise in temperature or due to replacement of transistor), V_{CE} decreases due to larger voltage drop across collector resistorR_C. The result is that base current $I_B$is reduced. The reduced base current in turn reduces the original increase in collector currentI_C. Thus a mechanism exists in the circuit which does not allow collector current I_C to increase rapidly.

Circuit Analysis

The required value of base current I_B to give zero signal collector current I_C can be determined as follows:



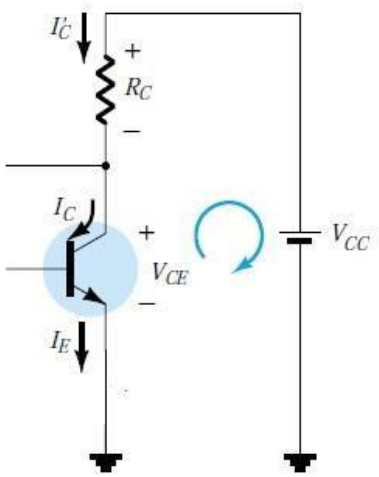
From the circuit diagram shown in Figure, applying Kirchhoff's voltage law to the input circuit, we have

$$V_{CC} - I_C'R_C - I_BR_B - V_{BE} = 0$$

$$V_{CC} - (I_B + I_C)R_C - I_BR_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE} - I_CR_C}{R_B + R_C}$$

From the output section of the circuit we have



$$V_{CE} = V_{CC} - I_C{}' R_C$$

Since $I_C{}' \cong I_C$

$$V_{CE} = V_{CC} - I_C R_C$$

This is exactly as obtained for fixed-bias configuration.

Stability Factors in Collector-to-Base Bias

S (I_{CO}):-

$$S(I_{CO}) = \frac{dI_C}{dI_{CO}} \quad Where\ V_{BE}\ and\ \beta\ are\ constant$$

From the input circuit we get

$$V_{CC} - I_B(R_C + R_B) - V_{BE} - I_C R_C = 0$$

Differentiating above w.r.t. I_C keeping V_{BE} as constant

$$\frac{dV_{cc}}{dI_C} - (R_c + R_B)\frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} - R_C = 0$$

$$\frac{dI_B}{dI_C} = \frac{-R_C}{R_B + R_C}$$

General expression for S (I_{CO}) is given by

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

So, the Stability Factor due to leakage current in collector-to-base bias circuit is

$$\boxed{S(I_{CO}) = \frac{1 + \beta}{1 + \beta \frac{R_C}{R_B + R_C}}}$$

Value of stability factor so obtained is less than (1+β) obtained from fixed-bias circuit. So this method provides improved stability as compared to that of fixed-bias circuit.

S (V_{BE}):-

$$S(V_{BE}) = \frac{dI_C}{dV_{BE}} \quad Where\ \beta\ and\ I_{CO}\ are\ constant$$

In collector-to-base bias circuit the input loop equation is given by

$$V_{CC} - I_B(R_C + R_B) - V_{BE} - I_C R_C = 0$$

$$V_{CC} - \frac{I_C}{\beta}(R_C + R_B) - V_{BE} - I_C R_C = 0$$

$$V_{CC} - I_C\left(\frac{R_C + R_B}{\beta} + R_C\right) - V_{BE} = 0$$

Differentiating above w.r.t. I_C keeping β as constant

$$\frac{dV_{cc}}{dI_C} - \left(\frac{R_c + R_B}{\beta} + R_C\right)\frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} = 0$$

So, the Stability Factor due to base emitter voltage in collector-to-base bias Circuit is

$$\boxed{S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_C}}$$

S (β):-

$$S(\beta) = \frac{dI_C}{d\beta} \quad Where\ V_{BE}\ and\ I_{CO}\ are\ constant$$

General expression for S (β) is given by

$$S(\beta) = \frac{I_{CO} + I_B}{1 - \beta\frac{dI_B}{dI_C}}$$

In collector-to-base bias circuit

$$\frac{dI_B}{dI_C} = \frac{-R_C}{R_B + R_C}$$

So, the Stability Factor due to current gain β in collector-to-base bias circuit is

$$S(\beta) = \frac{I_B + I_{CO}}{1 + \beta \dfrac{R_C}{R_B + R_C}}$$

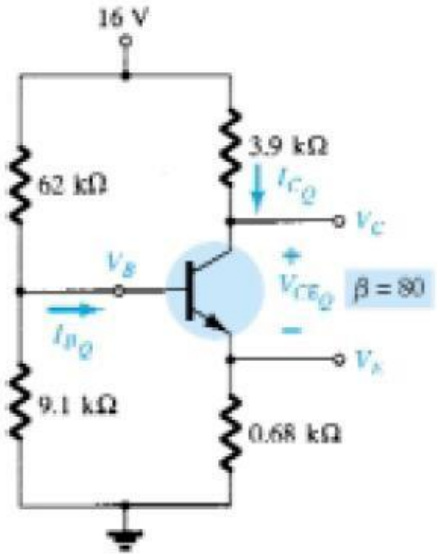
Numerical

1. For the network of Fig., determine:

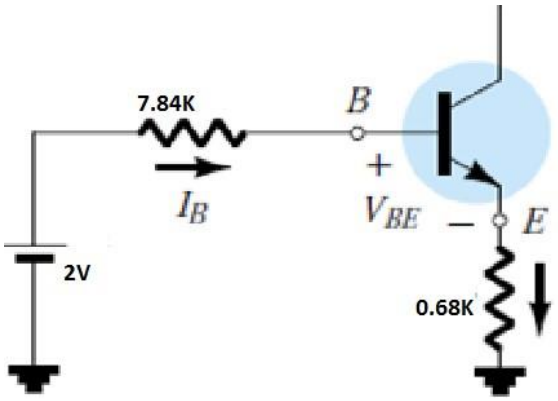
   (a) $S(I_{CO})$

   (b) $S(V_{BE})$

   (c) $S(\beta)$ Using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than$\beta(T_1)$.



a) Applying Thevenin equivalent results



From the input circuit we get

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_{Th} - V_{BE} - (I_B + I_C)\, R_E = 0$$

$$2V - I_B(7.84K) - 0.7 - (I_C + I_B)(0.68K) = 0$$

Differentiating above w.r.t. I_C keeping V_{BE} as constant

$$\frac{dV_{Th}}{dI_C} - R_{Th}\frac{dI_B}{dI_C} - \frac{dV_{BE}}{dI_C} - R_E\frac{dI_B}{dI_C} - R_E = 0$$

$$(-7.84K)\frac{dI_B}{dI_C} - (0.68K) - (0.68K)\frac{dI_B}{dI_C} = 0$$

$$-(8.52K)\frac{dI_B}{dI_C} = 0.68K$$

$$\frac{dI_B}{dI_C} = -7.98 \times 10^{-2}$$

$$S(I_{CO}) = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

$$= \frac{81}{1 + 80 \times 7.98 \times 10^{-2}} = 10.96$$

b) From the input circuit,

$$V_{Th} - \frac{I_C}{\beta} R_{Th} - V_{BE} - (\beta + 1) \frac{I_C}{\beta} R_E = 0$$

$$2 - \frac{I_C}{80}(7.84K) - V_{BE} - \frac{81 \times (0.68K)}{80} I_C = 0$$

By, differentiation

$$-(0.098K) - \frac{dV_{BE}}{dI_C} - (0.68K) = 0$$

$$S(V_{BE}) = -1.28 \times 10^{-3} s$$

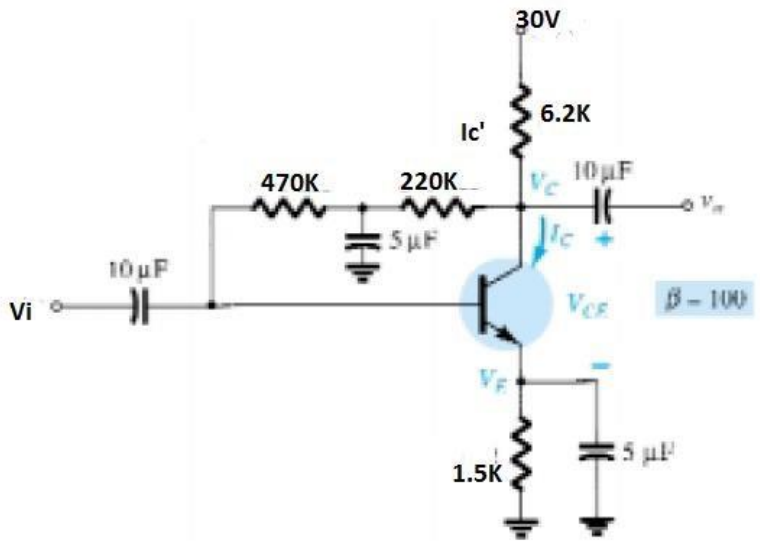
c) $\beta_1 = 80$ $\beta_2 = 80$

$I_{C1} = 1.653mA$ $I_{C2} = 1.698mA$

$$S(\beta) = \frac{1.698 - 1.653}{100 - 80} = 2.25 \times 10^{-6} A$$

2. For the voltage feedback network of Fig., determine:

a) I_C
b) V_C
c) V_E
d) V_{CE}



a) $30 - (6.2K)I_C{}' - (470K + 220K)I_B - 0.7 - (1.5K)I_E = 0$

$$30 - (6.2K)(\beta + 1)I_B - (690K)I_B - 0.7 - (1.5K)(\beta + 1)I_B = 0$$

$$30 - (6.2K) \times 101I_B - (690K)I_B - 0.7 - (1.5K) \times 101I_B = 0$$

$$I_B = 19.96\mu A$$

$$I_C = \beta I_B = 1.99mA$$

b) $30 - (6.2K)I_C{}' - V_C = 0$

$$V_C = 17.49V$$

c) $V_E = I_E R_E = 2.026 \times 1.5 = 3.024V$

d) $V_{CE} = V_C - V_E = 14.466V$

MOS
Field-Effect Transistor

Prepared by:

DEBASISH MOHANTA

Assistant Professor

Department of Electrical Engineering

GCE, Keonjhar

References: 1. "Electronic Devices and Circuits"

J.B. Gupta

2. "Semiconductor physics and devices"

Donald A. Neaman

3. "Microelectronics Circuits" Sedra and Smith

Field Effect Transistor

The field effect transistor is a semiconductor device, which depends for its operation on the control of current by an electric field. There are two of field effect transistors:

- ✓ JFET (Junction Field Effect Transistor)
- ✓ MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

The FET has several advantages over conventional transistor.

- ✓ In a conventional transistor, the operation depends upon the flow of majority and minority carriers. That is why it is called bipolar transistor.

In FET the operation depends upon the flow of majority carriers only. It is called unipolar device.

- ✓ The input to conventional transistor amplifier involves a forward biased PN junction with its inherently low dynamic impedance. The input to FET involves a reverse biased PN junction hence the high input impedance of the order of Mega ohm.

- ✓ It is less noisy than a bipolar transistor.
- ✓ It exhibits no offset voltage at zero drain current. ✓ It has thermal stability.
- ✓ It is relatively immune to radiation

Operation of JFET

Consider a sample bar of N-type semiconductor. This is called N-channel and it is electrically equivalent to a resistance as shown in **fig. 1**.

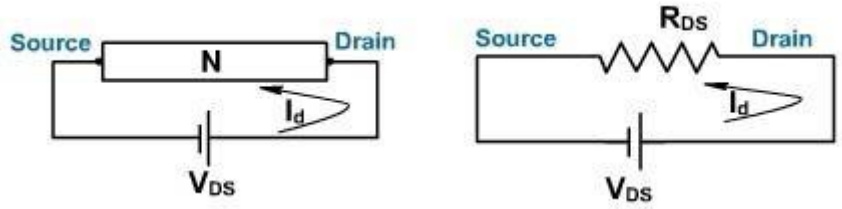


Fig. 1

Ohmic contacts are then added on each side of the channel to bring the external connection. Thus if a voltage is applied across the bar, the current flows through the channel.

The terminal from where the majority carriers (electrons) enter the channel is called source designated by S. The terminal through which majority carriers leave the channel is called drain and designated by D. For an N-channel device, electrons are the majority carriers. Hence the circuit behaves like a dc voltage V_{DS} applied across a resistance R_{DS}. The resulting current is the drain current I_D. If V_{DS} increases, I_D increases proportionally.

Now on both sides of the n-type bar heavily doped regions of p-type impurity have been formed by any method for creating pn junction. These impurity regions are called gates (gate1 and gate2) as shown in **fig. 2**.

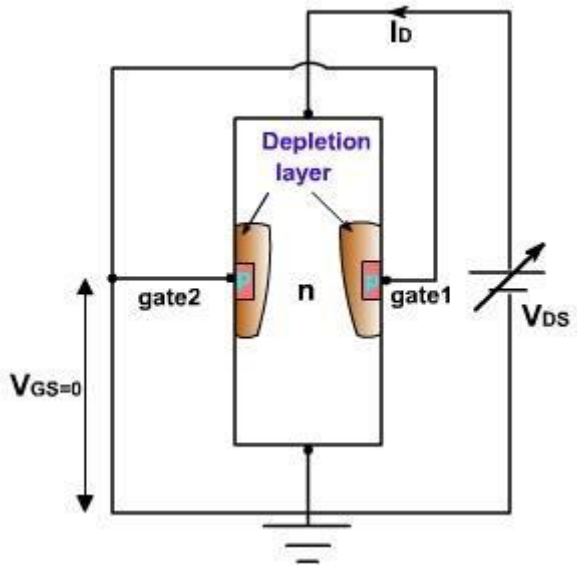


Fig. 2

Both the gates are internally connected and they are grounded yielding zero gate source voltage (V_{GS} =0). The word gate is used because the potential applied between gate and source controls the channel width and hence the current.

As with all PN junctions, a depletion region is formed on the two sides of the reverse biased PN junction. The current carriers have diffused across the junction, leaving only uncovered positive ions on the n side and negative ions on the p side. The depletion region width increases with the magnitude of reverse bias. The conductivity of this channel is normally zero because of the unavailability of current carriers.

The potential at any point along the channel depends on the distance of that point from the drain, points close to the drain are at a higher positive potential, relative to ground, then points close to the source. Both depletion regions are therefore subject to greater reverse voltage near the drain. Therefore the depletion region width increases as we move towards drain. The flow of electrons from source to drain is now restricted to the narrow channel between the no conducting depletion regions. The width of this channel determines the resistance between drain and source.

Characteristics of JFET

Consider now the behavior of drain current I_D vs drain source voltage V_{DS}. The gate source voltage is zero therefore V_{GS}= 0. Suppose that V_{DS} is gradually linearly increased linearly from 0V. I_D also increases.

Since the channel behaves as a semiconductor resistance, therefore it follows ohm's law. The region is called ohmic region, with increasing current, the ohmic voltage drop between the source and the channel region reverse biased the junction, the conducting portion of the channel begins to constrict and I_D begins to level off until a specific value of V_{DS} is reached, called the **pinch of voltage V_P**.

At this point further increase in V_{DS} does not produce corresponding increase in I_D. Instead, as V_{DS} increases, both depletion regions extend further into the channel, resulting in a no more cross section, and hence a higher channel resistance. Thus even though, there is more voltage, the resistance is also greater and the current remains relatively constant. This is called pinch off or saturation region. The current in this region is maximum current that FET can produce and designated by I_{DSS}. (Drain to source current with gate shorted).

As with all pn junctions, when the reverse voltage exceeds a certain level, avalanche breakdown of pn junction occurs and I_D rises very rapidly as shown in fig. 3.

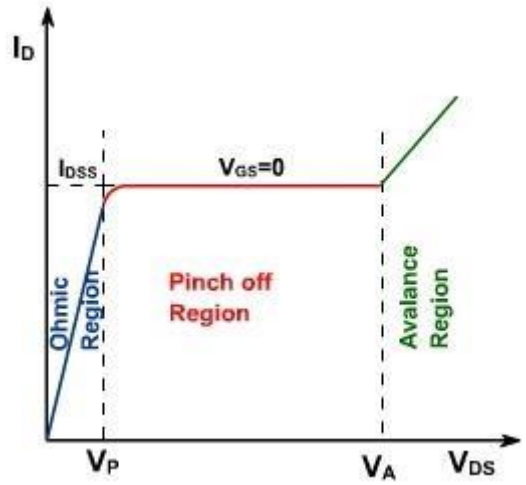


Fig. 3

Consider now an N-channel JFET with a reverse gate source voltage as shown in fig. 4.

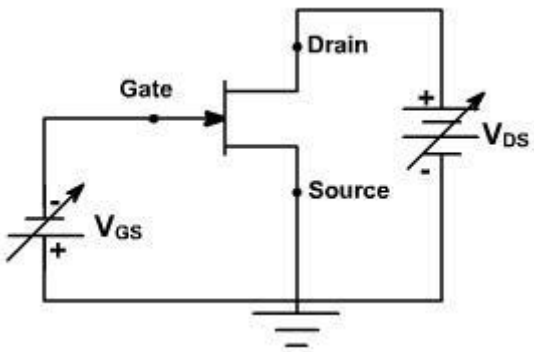


Fig.4

The additional reverse bias, pinch off will occur for smaller values of | V_{DS} |, and the maximum drain current will be smaller. A family of curves for different values of V_{GS} (negative) is shown in **fig. 5**.

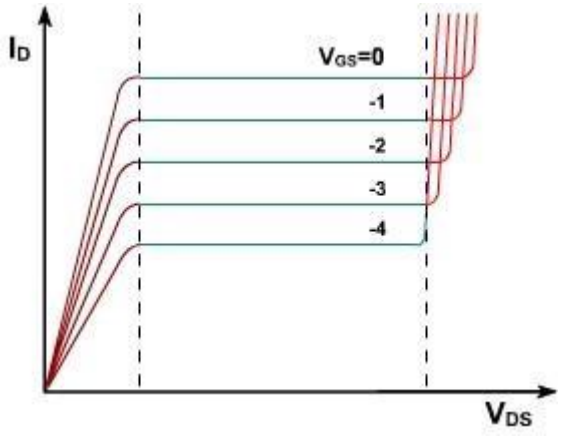


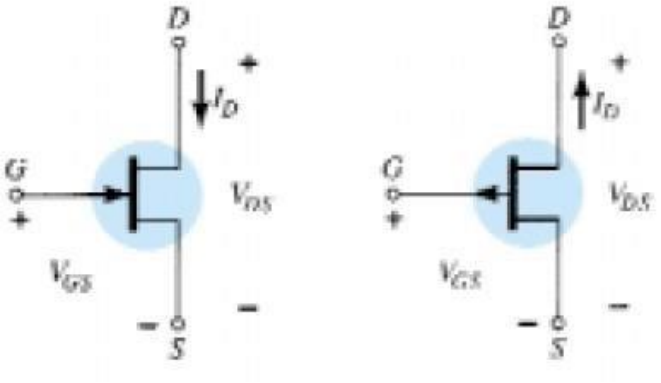
Fig.5

When the gate voltage is negative enough, the depletion layers touch each other and the conducting channel pinches off (disappears). In this case the drain current is cut off. The gate voltage that produces cut off is symbolized V_{GS} (off). It is same as pinch off voltage.

Since the gate source junction is a reverse biased silicon diode, only a very small reverse current flows through it. Ideally gate current is zero. As a result, all the free electrons from the source go to the drain i.e. $I_D = I_S$. Because the gate draws almost negligible reverse current the input resistance is very high 10's or 100's of M ohm. Therefore where high input impedance is required, JFET is preferred over BJT. The disadvantage is less control over output current i.e. FET takes larger changes in input voltage to produce changes in output current. For this reason, JFET has less voltage gain than a bipolar amplifier.

Symbol of JFET

The graphic symbols for the n-channel and p-channel JFETs are provided in Fig. Note that the arrow is pointing in for the n-channel device of Fig. to represent the direction in which $I_G$would flow if the p-n junction were forward-biased. For the p-channel device the only difference in the symbol is the direction of the arrow.



(a) n-channel (b) p-channel

JFET Temperature Effects

It is possible to bias the JFET such that it exhibits a zero temperature co-efficient i.e. drain current is independent of temperature. There are two mechanisms for controlling the temperature sensitivity of the conduction of a JFET channel.

- ✓ Decreasing the depletion region width at the channel-gate pn junction with increase in temperature, this result in increase in channel thickness.
- ✓ Decrease in carrier mobility with increase in temperature.

Increase in channel thickness with increasing temperature makes drain current I_D to increase. Another way of looking in to the situation is that, V_P increase in magnitude with increase in temperature. V_P has a positive temperature coefficient of about 2.2 mV/^{0}C.

The second factor, i.e. decrease in carrier mobility with increase in temperature make channel conductivity to decrease with increase in temperature. The result is that, the drain current decreases with increase in temperature.

So, we have two distinct mechanism effecting the $I_D$as a function of temperature. Since both these mechanisms occur simultaneously, it is possible to bias the JFET so as to exhibit zero temperature co-efficient. Thus the JFET have higher thermal stability as thermal runaway does not occur in JFET.

JFET Parameters

1. AC drain resistance

It is defined as the ratio of change in V_{DS} to the change in drain current at constant gatesource voltageV_{GS}. It is denoted as r_d.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad at\ constant V_{GS}$$

It is also called dynamic drain resistance and its value is very large from 10 KΩ to 1 MΩ.

2. Transconductance

The control that V_{GS}has over drain current $I_D$is measured by transconductance. It is denoted asg_m. It may be defined as ratio of change in drain current(I_D) to the change in gate-source voltage (V_{GS}) at constant drain-source voltage (V_{DS}).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|\, V_{DS} = constant$$

It is also called the forward trans-admittance (y_{fs}) or forward transconductance (g_{fs}). It is measured in $^{mA}/_{V}$ or milli siemens.

3. Amplification Factor

It may be defined as ratio of change in drain-source voltage (V_{DS}) to the change in gatesource voltage (V_{GS}) at constant drain current(I_D). It is denoted as μ.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\bigg|\, I_D = constant$$

Relationship among JFET parameters

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d \times g_m}$$

JFET Equation

The drain current $I_D$of JFET described by the following equation

$$\boxed{I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2}$$

MOSFET

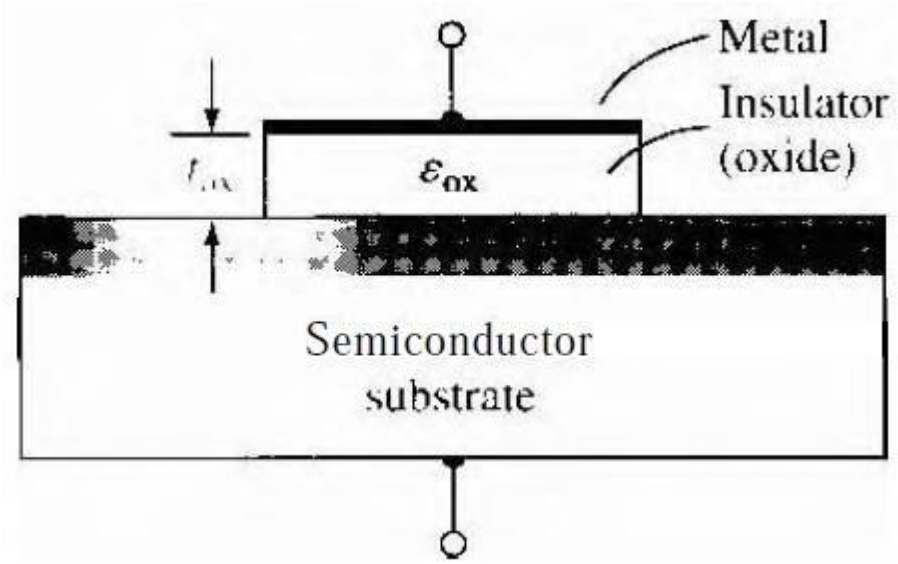
INTRODUCTION

- ✓ The metal-oxide-semiconductor field effect transistor (MOSFET) became a practical reality in the 1970s.
- ✓ The MOSFET compared to BJTs, can be made very small i.e. it occupies a very small area on an IC chip.
- ✓ Since digital circuits can be designed using only MOSFETs, with essentially no resistors or diodes required, high density VLSI circuits, including microprocessors and memories can be fabricated.
- ✓ The MOSFET has made possible the handheld calculator, the powerful personal computer and the laptop computer.

MOS STRUCTURE

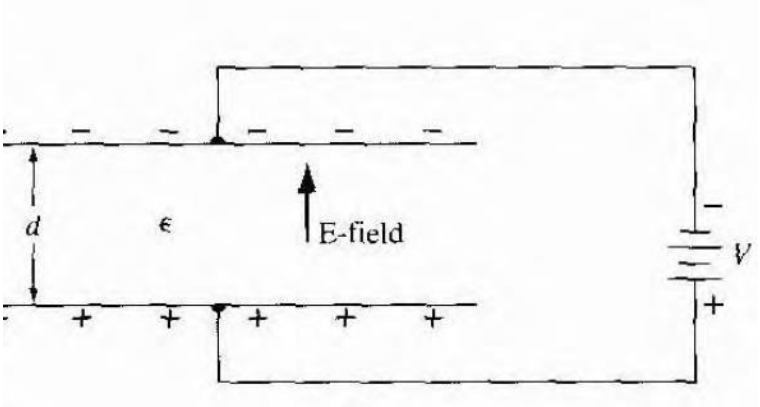
MOS Capacitor

- ✓ The heart of the MOSFET is the metal-oxide-semiconductor capacitor.
- ✓ The metal may be aluminium or some other type of metal.
- ✓ In most cases, the metal is replaced by a high conductivity polycrystalline silicon layer deposited on oxide.
- ✓ However the term metal is usually still used in referring to MOSFETs.
- ✓ The parameter t_{ox} is the thickness of the oxide and $\in_{ox}$ is the oxide permittivity.

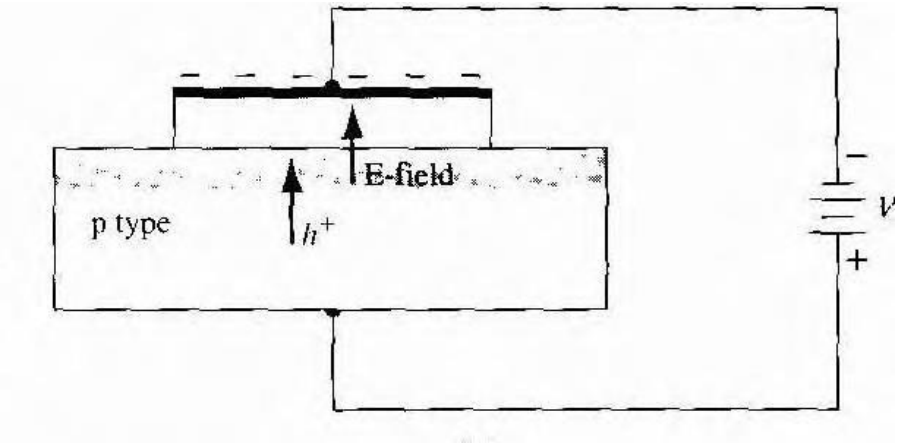


Parallel plate capacitor

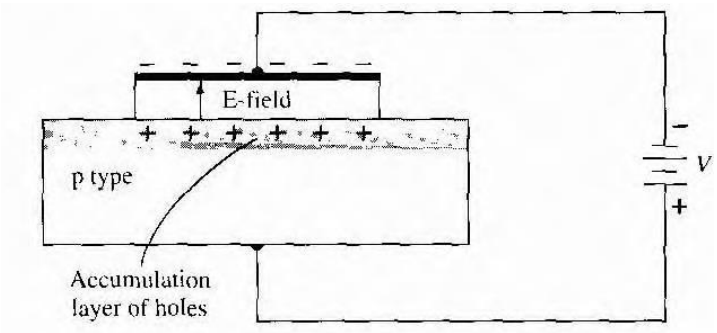
- ✓ The physics of MOS structure can be explained with the aid of a simple parallel plate capacitor.
- ✓ Figure shows a parallel plate capacitor with the top plate at negative voltage w.r.t. the bottom plate.
- ✓ An insulator material separates two plates.
- ✓ With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate and electric field is induced between the two plates.



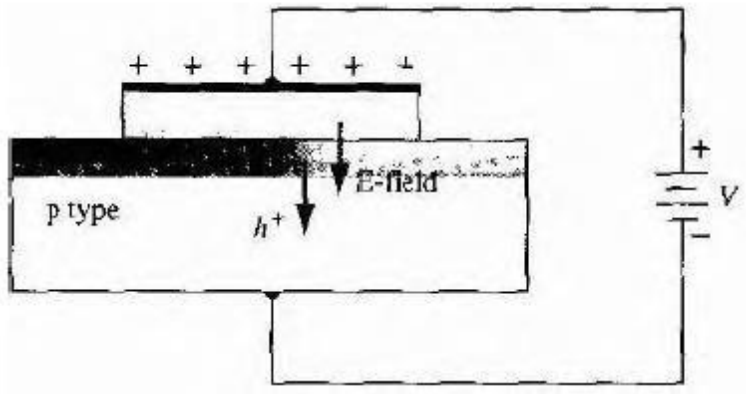
MOS capacitor with p-type Substrate



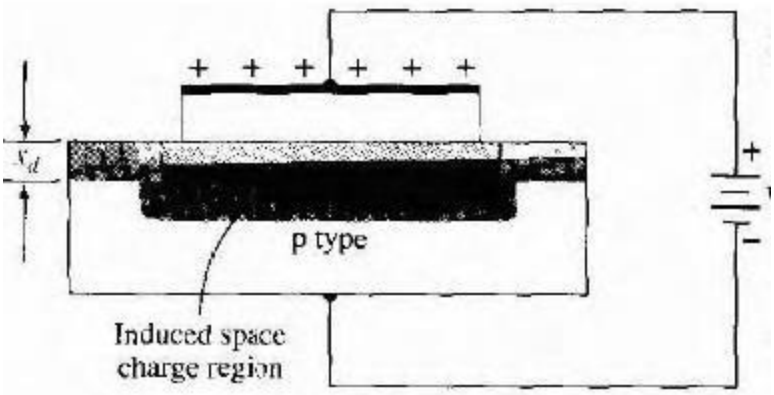
- ✓ Figure shows an MOS capacitor with a p-type semiconductor substrate.
- ✓ The top metal gate is at a negative voltage with respect to the semiconductor substrate.
- ✓ From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced with the direction shown in the figure.
- ✓ If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide-semiconductor interface.



- ✓ An ***accumulation layer of holes*** in the oxide-semiconductor junction corresponds to the positive charge on the bottom "plate" of the MOS capacitor.
- ✓ Figure shows the same MOS capacitor in which the polarity of the applied voltage is reversed.



- ✓ A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction as shown.
- ✓ If the electric field penetrates the semiconductor in this case, majority carrier holes will experience a for away from the oxide-semiconductor interface.
- ✓ As the holes are pushed away the interface, a negative space charge region is created because of the fixed acceptor impurity atoms.
- ✓ The negative charge in the induced depletion region corresponds to the negative charge on the bottom "plate" of the MOS capacitor.

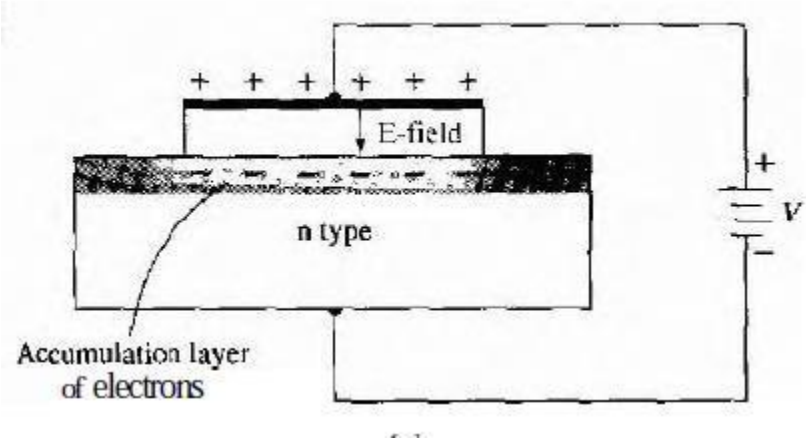


- ✓ When a large positive voltage is applied to the gate, the magnitude of the induced electric field increases.
- ✓ Minority carrier electrons are attracted to the oxide-semiconductor interface.
- ✓ This region of minority carrier electrons is called an *electron inversion layer*.

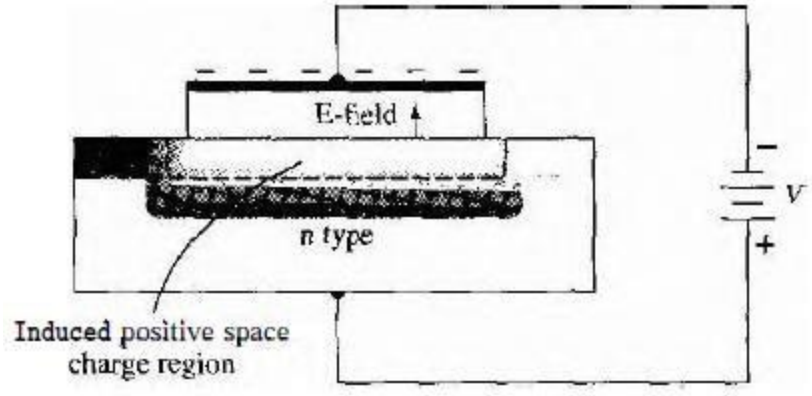
MOS capacitor with n-type Substrate

- ✓ The top metal plate is at positive voltage w.r.t. the semiconductor interface.
- ✓ A positive charge is created on the top plate and electric field is induced.

- ✓ In this situation an accumulation layer of electrons is induced in the n-type semiconductor.



- ✓ When a negative voltage is applied to the gate terminal, a positive space charge region is induced in the n-type substrate by the induced electric field.
- ✓ When a large negative voltage is applied, a region of positive charge is created at the oxide semiconductor interface.
- ✓ This region of minority carrier holes is called *hole inversion layer*.

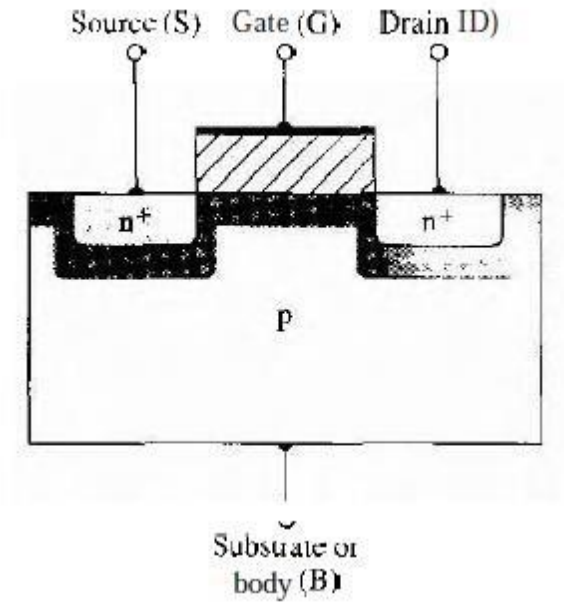


Enhancement-mode MOSFET

- ✓ The term enhancement mode means that a voltage must be applied to the gate to create an inversion layer.
- ✓ For MOS capacitor with a p-type substrate, a positive gate voltage must be applied to create the electron inversion layer.
- ✓ For MOS capacitor with a n-type substrate, a negative gate voltage must be applied to create the hole inversion layer.

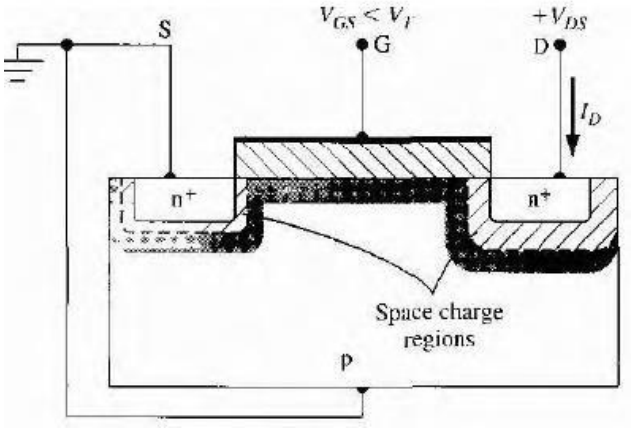
n-channel Enhancement-mode MOSFET

The gate, oxide and p-type substrate regions are same as those of a MOS capacitor. In addition, we have now two n-regions, called source terminal and drain terminal. The current in a MOSFET is the result of the flow of charge in the inversion layer, also called channelregion, adjacent to the oxide-semiconductor interface. The channel length of a typically integrator circuit MOSFET is less than 1µm which means MOSFETs are small devices. The oxide thickness t_{ox} is typically in the order of $400A^0$ or less. With zero bias applied to the gate, the source and drain terminals are separated by p-regions. This is equivalent to two back to back diodes. The current in this case is essentially zero. If large enough positive gate voltage is applied, an electron inversion layer is created at the oxide-semiconductor interface and this layer connects n-source to n-drain. A current can be generated between the source and drain terminals. Since a voltage must be applied to the gate to create the inversion charge, this transistor is called enhancement mode MOSFET. Since carriers in the inversion layer are electrons, this device is also called an n-channel MOSFET (NMOS). The source terminal supplies the electrons that flow through the channel and the drain terminal allows the carriers to drain from the channel. For n-channel MOSFET, electrons flow from the source to the drain with an applied drain-to-source voltage which means conventional current enters the drain and leaves the source. The magnitude of current is a function of the amount of the charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a spacecharge region, there is no current through the substrate.



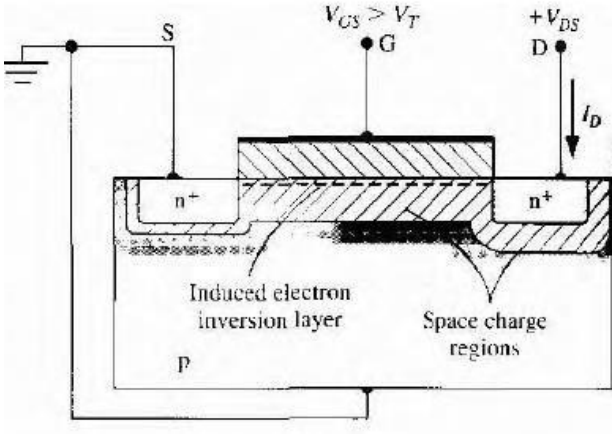
V-I Characteristics-NMOS Device

The threshold voltage of the n-channel MOFET, denoted asV_{TN}, is defined as the applied gate voltage needed to create an inversion layer. In simple terms, the threshold voltage is the gate voltage required to turn on the transistor. For the n-channel E-MOSFET, the threshold voltage is positive because a positive gate voltage is required to create the inversion layer. If the gate voltage is less than threshold voltage, the current in the device is essentially zero.

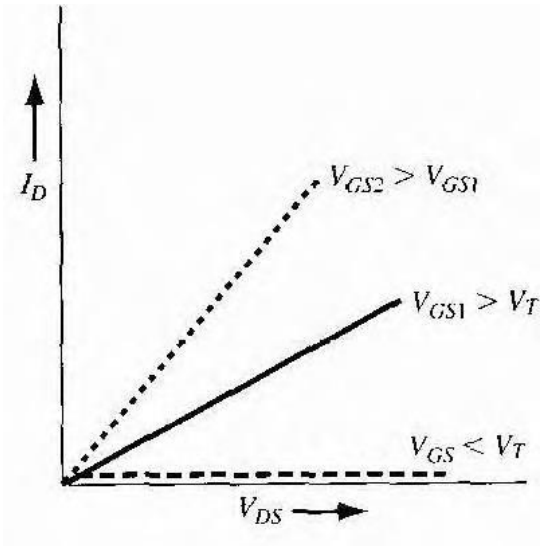


If the gate voltage is greater than the threshold voltage a drain-to-source current is generated as drain-to-source voltage is applied. The gate and drain voltages are measured w.r.t. the source. The drain-to-source voltage is less than threshold voltage and there is a small drain-to-source voltage. There is no electron in the inversion layer, the drain-tosubstrate pn junction is reverse biased and the drain current is zero. If the applied gate voltage is greater than the threshold voltage an electron inversion layer is created. When a small drain voltage is applied, electrons in the inversion

layer flow from source to positive drain terminal. The conventional current enters the drain terminal and leaves the source terminal. Note that positive drain voltage creates a reverse-biased drain-to-substrate pn junction, so current flows through the channel region and not through a pn junction.



The I_D versus V_{DS} characteristics, for small values of V_{DS}, are shown in Figure



When$V_{GS} < V_{TN}$, the drain current is zero. As V_{GS} becomes larger than V_{TN}, channel inversion charge density increases, which increases the channel conductance.

Figure shows the basic MOS structure for the case when $V_{GS} > V_{TN}$, and the applied V_{DS} voltage is small. The thickness of the inversion channel layer in the figure qualitatively indicates the relative charge density, which is essentially constant along the entire channel length for this case. The corresponding I_D versus V_{DS} curve is shown in the figure.

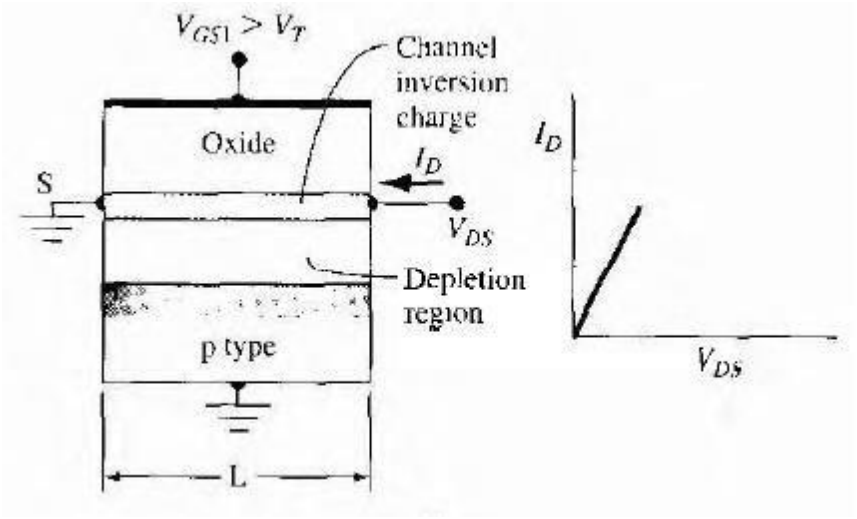
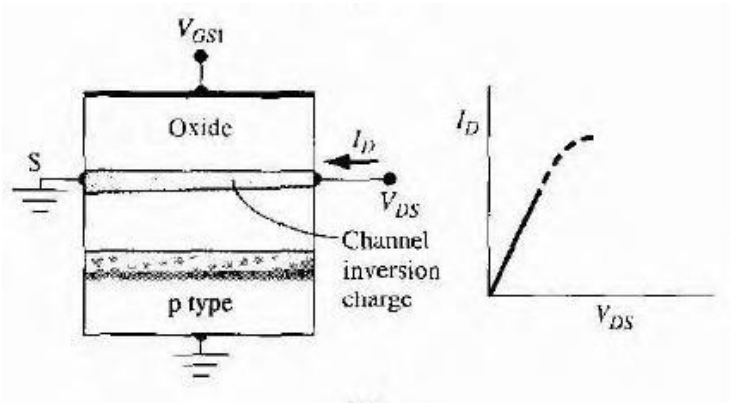


Figure shows the situation when the V_{DS} value increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain decreases, which means that the slope of the I_D versus V_{DS} curve will decrease. This effect is shown in the I_D versus V_{DS} curve in the figure.

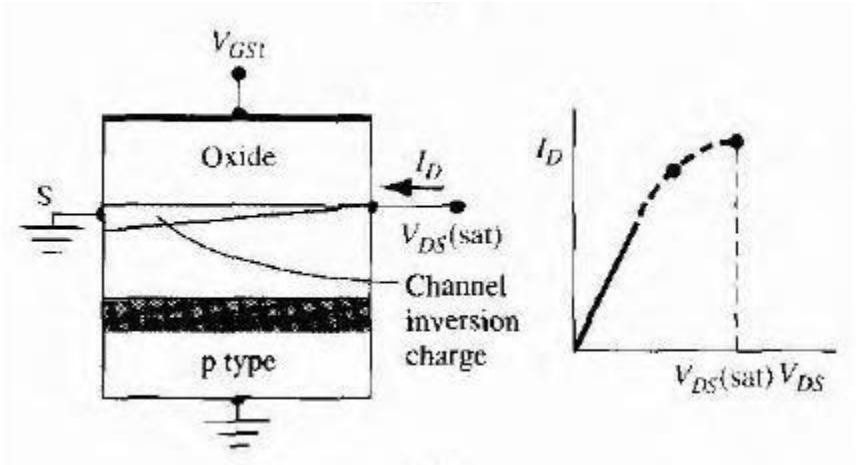


When V_{DS} increases to the point where the potential drop across the oxide at the drain terminal is equal to V_{TN}, the induced inversion charge density is zero at the drain terminal. This effect is schematically shown in Figure. At this point, the incremental conductance at the drain is zero, which means that the slope of the I_D versus V_{DS} curve is zero. We can write

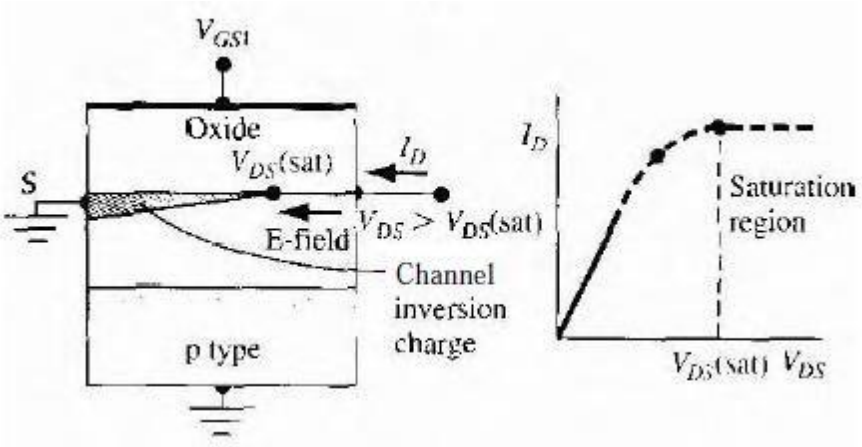
$$V_{GS} - V_{DS}(sat) = V_{TN}$$

Or, $$\boxed{V_{DS}(sat) = V_{GS} — V_{TN}}$$

where V_{DS}(sat) is the drain-to-source voltage producing zero inversion charge density at the drain terminal.



When V_{DS} becomes larger than the V_{DS} (sat) value, the point in the channel at which the inversion charge is just zero moves toward the source terminal. In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, the electrons are injected into the space charge region where they are swept by the E-field to the drain contact. If we assume that the change in channel length is small compared to the original length, then the drain current will be a constant for $V_{DS} > V_{DS}$ (sat). The region of the I_D versus V_{DS} characteristic is referred to as the ***saturation region.*** Figure shows this region of operation.



As the applied gate-to-source voltage changes, the I_D versus V_{DS} curve changes. The region for which $V_{DS} < V_{DS}(sat)$ is known as the ***non-saturation or triode region***. The ideal current-voltage characteristics in this region are described by the equation.

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

In the saturation region, the ideal current-voltage characteristics in this region are described by the equation.

$$I_D = K_n(V_{GS} - V_{TN})^2$$

$K_n$is the transconductance parameter which is given by:

$$K_n = \frac{\mu n C_{ox} W}{2L}$$

Where,

μ_n = mobility of electrons

C_{ox} = oxide capacitance

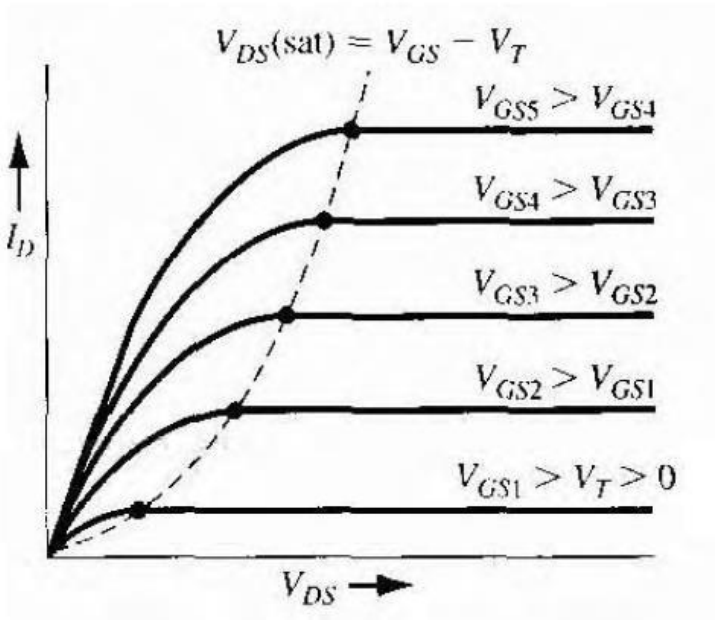
W= width of the channel

L= length of the channel

K_n' = process conduction parameter

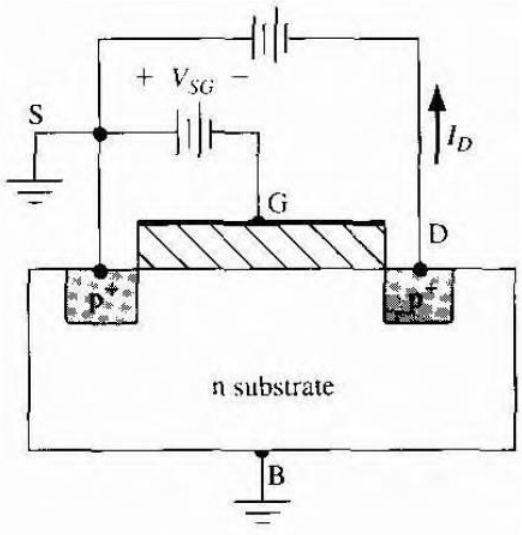
$$K_n' = \mu n C_{ox}$$

$$\frac{W}{L} = aspect\ ratio$$



p-channel Enhancement-mode MOSFET

The substrate is now n-type and the source and drain areas are p-type. The operation of pchannel device is same as n-channel device, except the hole is the charge carrier rather than the electron. A negative gate bias is required to induce an inversion layer of holes in the channel region directly under the oxide. The threshold voltage for p-channel device is denoted as V_{TP}. Since the threshold voltage is defined as the gate voltage required to induce the inversion layer, then $V_{TP} < 0$ for p-channel enhancement-mode device.



Once the inversion layer has been created, the p-type source region is the source of the charge carrier so that holes flow from the source to drain. A negative drain voltage is therefore required to induce an E-field in the channel forcing the holes to move from the source to drain. The conventional current direction, then for pMOS transistor is in to the source and out of drain. The voltage polarities and current direction are the reverse of those in the n-channel device. We may note the change in the subscript notation for this device. V_{SD}(sat) the drain-to-source voltage producing zero inversion charge density at the drain terminal is given by

$$V_{SD}(sat) = V_{SG} + V_{TP}$$

The ideal current-voltage characteristics in non-saturation region are described by the equation.

$$I_D = K_n[2(V_{SG} + V_{TP})V_{SD} - {V_{SD}}^2]$$

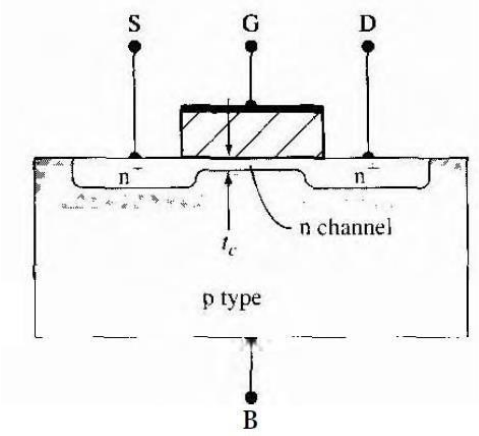
In the saturation region, the ideal current-voltage characteristics in this region are described by the equation.

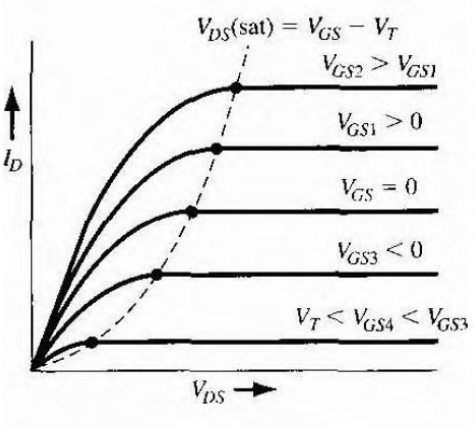
$$I_D = K_n(V_{SG} + V_{Tp})^2$$

Depletion-mode MOSFET

n-channel DMOSFET

When zero volts applied to the gate, an n-channel region or inversion layer exists under the oxide. Since an n-region connects the n-source and n-drain, a drain-to-source current may be generated in the channel even with zero gate voltage. The term depletion mode means that a channel exists even at zero gate voltage. A negative gate voltage must be applied to the nchannel D-MOSFET to turn the device off. A negative gate voltage induces a space charge region under the oxide, thereby reducing the thickness of the n-channel oxide. The reduced thickness decreases the channel conductance, which in turn reduces the drain current. The more negative the gate voltage the less is the drain current.





- ✓ The device is normally ON, we need to provide bias to turn off or pinch off the channel.

D-MOSFET Vs. E-MOSFET

D-MOSFET

- ✓ Normally ON MOSFET
- ✓ Already there is a channel in case of D-MOSFET.
- ✓ Increasing the magnitude of gate bias decreases the current.

E-MOSFET

- ✓ Normally OFF MOSFET
- ✓ There is no channel in first initially.
- ✓ Increasing the magnitude of gate bias increases the current.
- ✓ It is normally conducting but becomes non conducting as the carriers are depleted or pulled from the channel by applying voltage.

N-channel Vs. P- channel MOSFET

- ✓ It is normally non conducting but becomes conducting when the channel is enhanced by applying voltage.
- ✓ To turn ON the channel, we need to provide bias the gate higher than the threshold voltage.
- ✓ P-channel is much easier and cheaper to produce than N-channel device.
- ✓ N-channel MOSFET is smaller for the same complexity than that of P-channel MOSFET.
- ✓ N-channel MOSFET has faster switching operation than P-channel MOSFET.

- ✓ P-channel occupies larger area than N-channel for given drain current rating because the electron mobility is 2.5 times more than that of holes.

- ✓ The drain resistance of P-channel MOSFET is three times higher than that of an identical N-channel MOSFET.

Numericals

1. Use the expression for operation in triode region to show that an N-channel MOSFET operated with an overdrive voltage $V_{OV} = V_{GS} - V_{tN}$ and having small V_{DS}across it behaves approximately as a linear resistance,

$$r_{DS} = \frac{1}{[K_n' \frac{W}{L} V_{ov}]}$$

Obtained for a device having $K_n' = 1000\ {}^{\mu A}/_{V^2}$ and $\frac{W}{L} = 10$; when operated with an overdrive voltage of 0.5V.

Solution:

In triode region,

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - {V_{DS}}^2]$$

Taking, ${V_{DS}}^2$ very negligible due to very small value,

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS}]$$

$$r_{DS} = (\frac{\partial I_D}{\partial V_{DS}})^{-1} \Big| V_{DS} = constant$$

$$\frac{\partial I_D}{\partial V_{DS}} = K_n[2(V_{GS} - V_{TN})] = K_n 2\, V_{OV}$$

$$r_{DS} = \frac{1}{K_n 2\, V_{OV}}$$

$$= \frac{1}{[\mathrm{K_n}' \frac{\mathrm{W}}{\mathrm{L}} \mathrm{V_{OV}}]}$$

$$r_{DS} = \frac{1}{100 \times 10^{-6} \times 10 \times 0.5} = 20\mathrm{k}\Omega$$

2. For a $0.5\mu m$ process technology, for which $t_{ox} = 15\ nm$ & $\mu_n = 550^{cm_2}/s$. Find C_{ox}, $\mathrm{K_n}'$ and over drive voltage $V_{OV} = V_{GS} - V_{tN}$ required to operate a transistor having $\frac{\mathrm{W}}{\mathrm{L}} = 20$ in saturation region with $I_D = 0.2mA$. What the minimum value is of V_{DS}required?

Solution:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\epsilon_{ox} = 3.9\epsilon_o = 3.9 \times 8.85 \times 10^{-14}$$

$$C_{ox} = \frac{3.45 \times 10^{-11}}{15 \times 10^{-9}} = 2.3\, {fF}/{\mu m^2}$$

$$\mathrm{K_n}' = \mu_n \mathrm{C_{ox}} = 127\ \mu\mathrm{A/V^2}$$

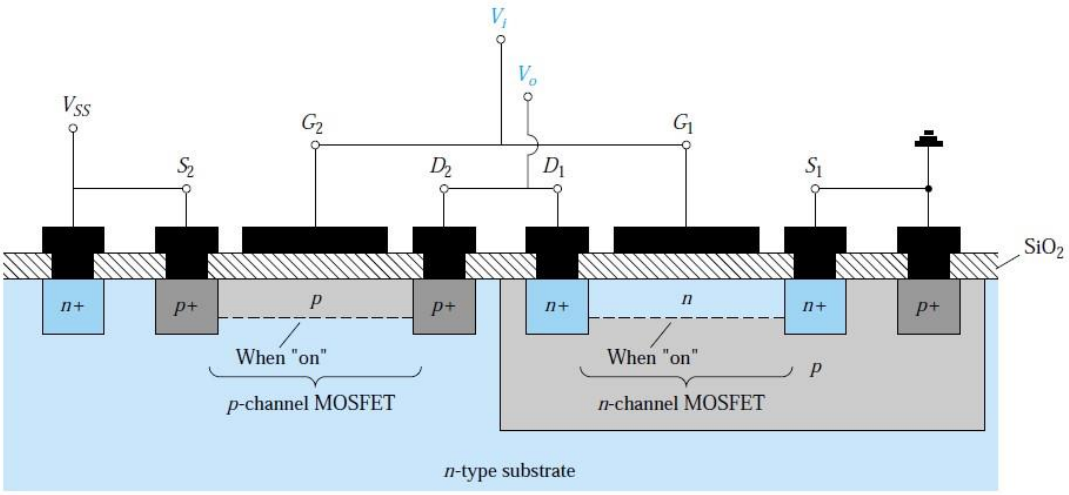
$$I_D = K_n (V_{GS} - V_{TN})^2$$

$$K_n = \frac{\mathrm{K_n}' W}{2L} = 1270\, {\mu\mathrm{A}}/{\mathrm{V^2}}$$

$$V_{OV} \equiv V_{GS} - V_{tN} = \sqrt{\frac{I_D}{K_n}} = \sqrt{\frac{0.2 \times 10^{-3}}{1270 \times 10^{-6}}} = 0.4V$$

Complimentary MOS

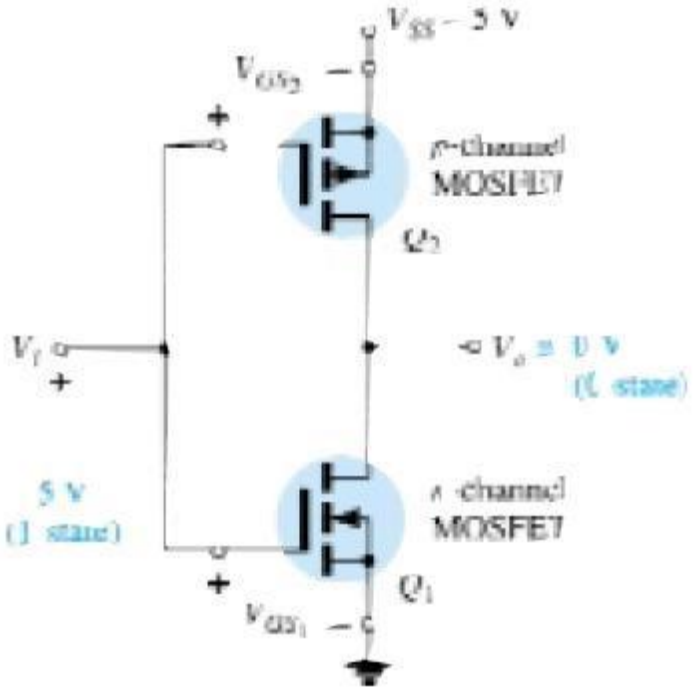
- ✓ A very effective logic circuit can be established by constructing a p-channel and an n-channel MOSFET on the same substrate as shown in Fig.
- ✓ The induced p-channel on the left and the induced *n*-channel on the right for the p- and n-channel devices, respectively.
- ✓ The configuration is referred to as a complementary MOSFET arrangement (CMOS) that has extensive applications in computer logic design.
- ✓ The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as CMOS logic design.



- ✓ One very effective use of the complementary arrangement is as an inverter, as shown in Fig.

- ✓ As introduced for switching transistors, an inverter is a logic element that "inverts" the applied signal.

- ✓ That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa.



- ✓ Both the gates are connected to the applied signal and both drain to the outputV_0.

- ✓ The source of the p-channel MOSFET (Q_2) is connected directly to the applied voltageV_{SS}, while the source of the *n*-channel MOSFET (Q_1) is connected to ground.

THE MOSFET AS AN AMPLIFIER AND AS A SWITCH

The basis for this important MOSFET application is that when operated in the saturation region, the MOSFET acts as a voltage-controlled current source: Changes in the gate-tosource voltage V_{GS} gives rise to drain currentI_D . Thus the saturated MOSFET used to implement a transconductance amplifier. However, since we are interested in linear amplification—that is, in amplifiers whose output signal (in this case, the drain currentI_D) is linearly related to their input signal (in this case, the gate-to-source voltageV_{GS})—we will have to find a way around the highly nonlinear (square-law) relationship ofI_D toV_{GS}.

The technique we will utilize to obtain linear amplification from a fundamentally nonlinear device is that of **dc biasing** the MOSFET to operate at a certain appropriate $V_{GS}$and a correspondingI_D) and then superimposing the voltage signal to be amplified, V_{GS}, on the dc bias voltage V_{GS}. By keeping the signal v_{gs}"small," the resulting change in drain current, i_d), can be made proportional tov_{gs}. We will study the total or large-signal operation of a MOSFET amplifier. We will do this by deriving the voltage transfer characteristic of a commonly used MOSFET amplifier circuit. From the voltage transfer characteristic we will be able to clearly see the region over which the transistor can be biased to operate as a smallsignal amplifier as well as those regions where it can be operated as a switch (i.e., being either fully "on" or fully "off"). MOS switches find application in both analogue and digital circuits.

Large-Signal Operation-The Transfer Characteristic

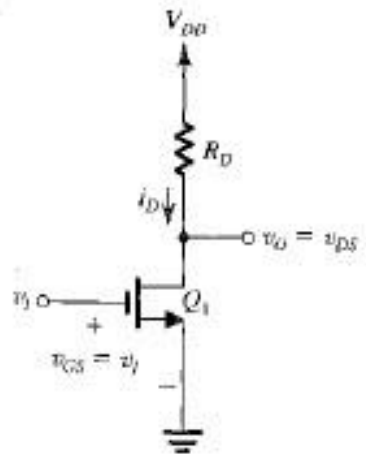


Figure shows the basic structure (skeleton) of the most commonly used MOSFET amplifier, the **common-source (CS)** circuit. The name common-source or **grounded-source** circuit arises because when the circuit is viewed as a two-port network, the grounded source terminal is common to both the input port, between gate and source, and the output port, between drain and source. Note that although the basic control action of the MOSFET is that changes in v_I as $v_{GS} = v_I$ give rise to changes ini_D**,** we are using a resistor R_D to obtain an output voltage v_0

$$v_0 = v_{DS} = v_{DD} - i_D R_D$$

In this way the transconductance amplifier is converted into a voltage amplifier. Finally, note that of course a dc power supply is needed to turn the MOSFET on and to supply the necessary power for its operation.

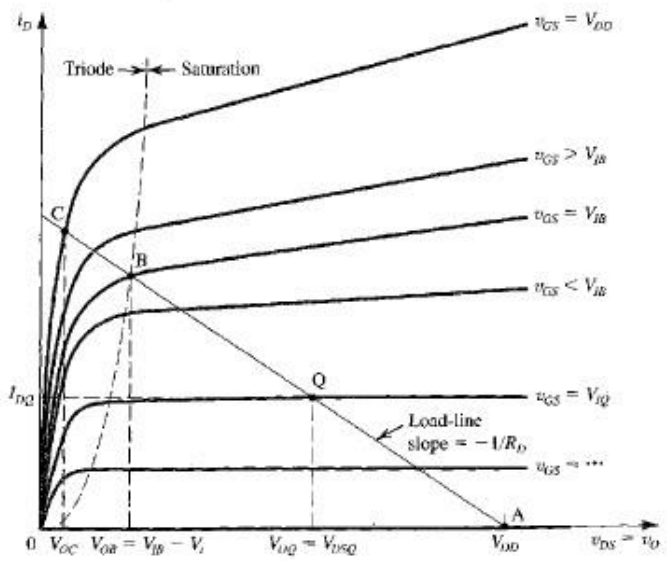
Graphical Derivation of the Transfer Characteristic

The operation of the common-source circuit is governed by the MOSFETs $i_D \sim v_{DS}$characteristics and by the relationship between $i_D and\ v_{DS}$imposed by connecting the drain to the power supply V_{DD} via resistorR_D, namely

$$v_{DS} = v_{DD} - i_D R_D$$

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS}$$

Figure shows a sketch of the MOSFETs $i_D \sim v_{DS}$ characteristic curves superimposed on which is a straight line representing the $i_D \sim v_{DS}$ relationship of Eq. Observe that the straight line intersects the v_{DS} -axis at V_{DD} [since from Eq. $v_{DS} = V_{DD}$ at$i_D = 0$] and has a slope of$-1/R_D$. Since R_D is usually thought of as the **load resistor** of the amplifier (i.e., the resistor across which the amplifier provides its output voltage), the straight line in Fig. is known as the **load line.**



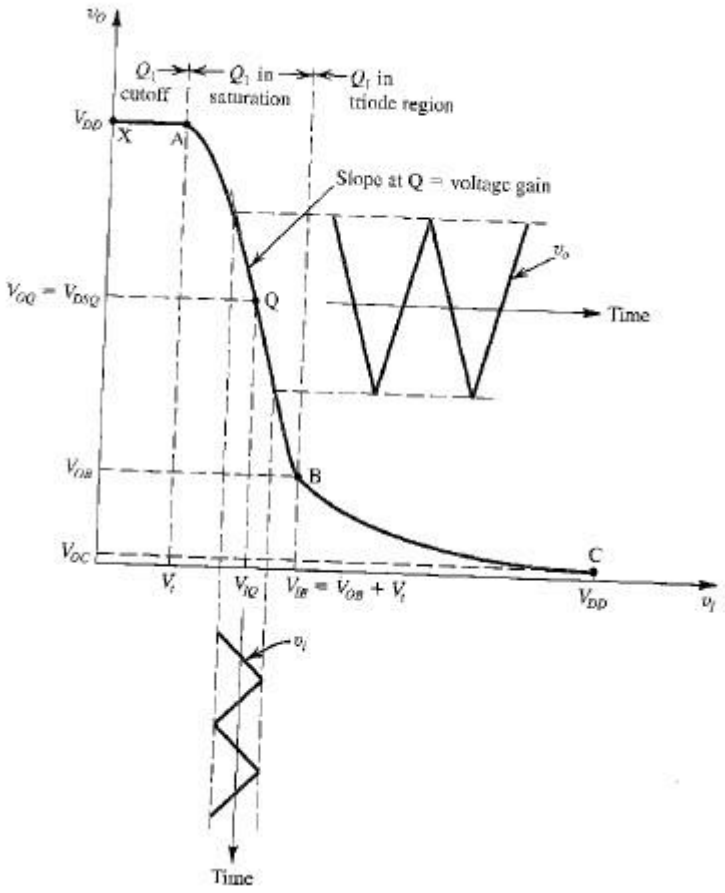
The graphical construction of Fig. can now be used to determine v_0(equal tov_{DS}) for each given value ofv_I ($v_{GS} = v_I$). Specifically, for any given value ofv_I . , we locate the corresponding i_D~v_{DS} curve and find v_0 from the point of intersection of this curve with the load line.

Qualitatively, the circuit works as follows: Since $v_{GS} = v_I$ we see that for$v_I < V_t$, the transistor will be cut off, $i_D$will be zero, and$v_0 = v_{DS} = v_{DD}$. Operation will be at the point labelled A. As v_I exceeds V_t, the transistor turns on, i_D increases, and v_0 decreases. Since$v_0$will initially be high, the transistor will be operating in the saturation region. This corresponds to points along the segment of the load line from A to B. We have identified a particular point in this region of operation and labelled it Q. It is obtained for $v_{GS} = v_{IQ}$and has the coordinates and$v_{OQ} = v_{DSQ} and\ i_{DQ}$

Saturation-region operation continues until v_0 decreases to the point that it is below v_I

by V_t, volts. At this point$v_{DS} = v_{GS} - V_t$, and the MOSFET enters its triode region of operation. This is indicated in Fig. by point B, which is at the intersection of the load line and the broken-line curve that defines the boundary between the saturation and the triode regions.

For$v_I > V_t$, the transistor is driven deeper into the triode region. Note that because the characteristic curves in the triode region are bunched together, the output voltage decreases slowly towards zero. Here we have identified a particular operating point C obtained for$v_I = v_{DD}$. The corresponding output voltageV_{OC}will usually be very small. This point-by point determination of the transfer characteristic results in the transfer curve shown in Fig. Observe that we have delineated its three distinct segments, each corresponding to one of the three regions of operation of MOSFETQ_1.



Operation as a Switch

When the MOSFET is used as a switch, it is operated at the extreme points of the transfer curve. Specifically, the device is turned off by keeping$v_I < V_t$, resulting$v_0 = V_{DD}$. The switch is turned on by applying a voltage closer toV_{DD}. Indeed, the common-source MOS circuit can be used as a logic inverter with the "low" voltage level close to 0 V and the "high" level close toV_{DD}.

Biasing of FETs and MOSFETs

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References: 1. "Electronic Devices and Circuit Theory"

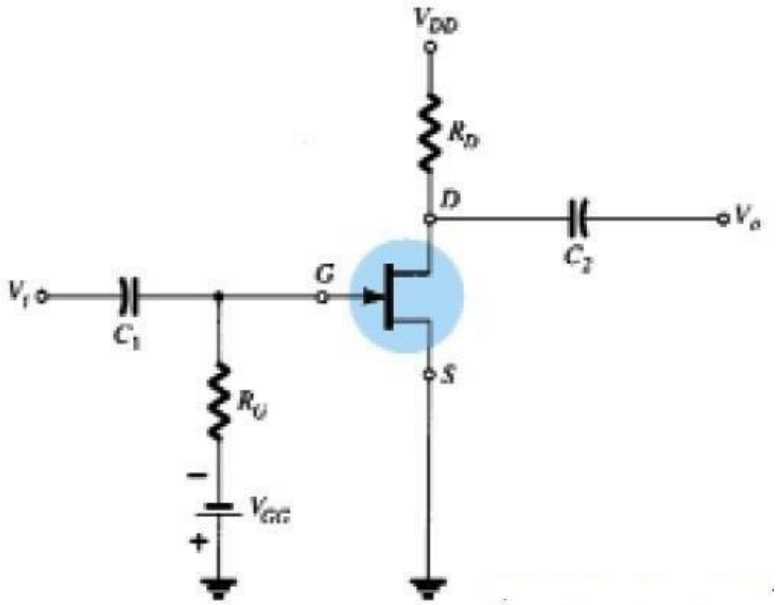
Robert L. Boylestad and L. Nashelsky

2. "Electronic Devices and Circuits"

J.B. Gupta

FET biasing

Fixed bias Configuration

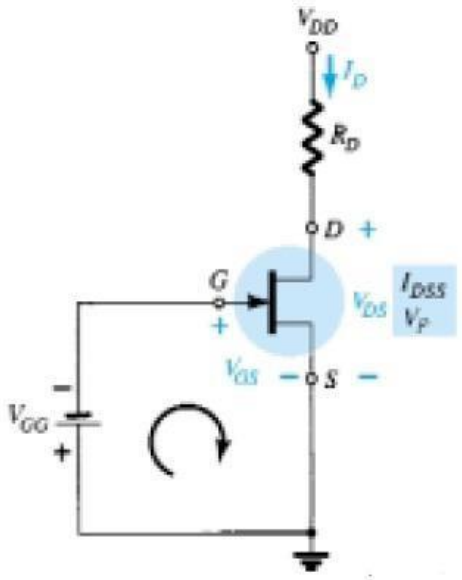


- ✓ Dc bias of a FET device needs setting of V_{GS} to give desiredI_D.

- ✓ For a JFET, drain current is limited by the saturation currentI_{DSS}.

- ✓ Since the JFET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a fixed battery voltage.

- ✓ Fixed dc bias is obtained using a batteryV_{GG}. This battery ensures that the gate is always negative w.r.t. the source and no current flows through the resistor R_G and gate terminal i.e. $I_G = 0$. The battery provides a voltage V_{GS} to bias the n-channel JFET, but no resulting current is drawn from the batteryV_{GG}. The dc voltage drop across R_G is equal to $I_G R_G$ i.e. 0 volt.



- ✓ The gate-source voltage V_{GS} is then

$$V_{GS} = V_G — V_S = — V_{GG}$$

- ✓ The gate-source current I_D is then fixed by the gate-source voltage as determined by the equation

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

- ✓ This current then causes a voltage drop across the drain resistor R_D and is given by

$$V_{RD} = I_D R_D$$

And the output voltage

$$V_D = V_{DD} - I_D R_D$$

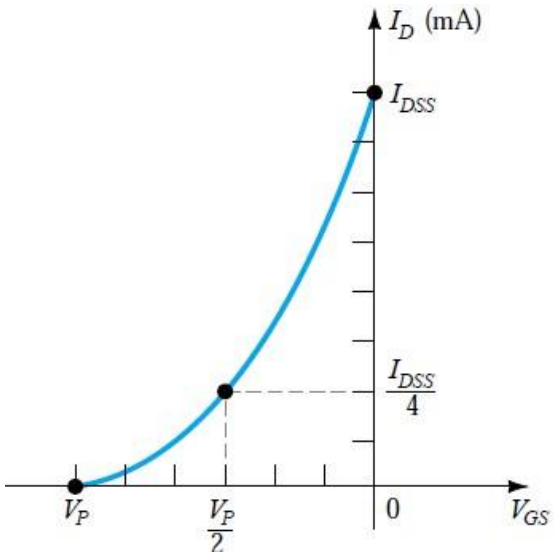
- ✓ Since V_{GG} is fixed value of dc supply and the magnitude of V_{GS} is also fixed, hence the circuit is named as fixed-bias circuit.

- ✓ Since this bias circuit uses two batteries V_{GG} and V_{DD}, it is also known as two battery bias circuit.

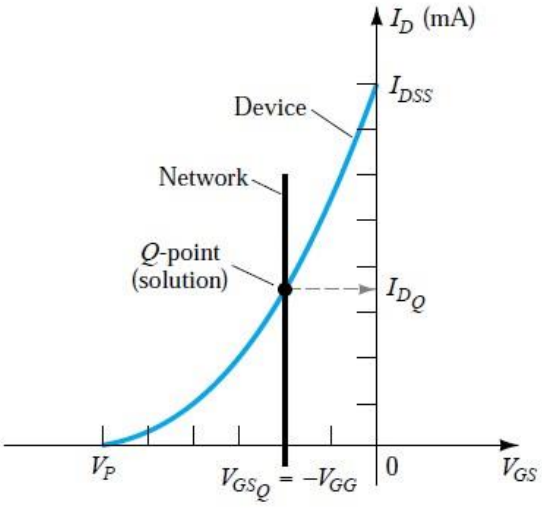
- ✓ A FET has high input impedance. To make advantage of it, R_G should be as large as possible so that input impedance of the circuit remains high. A reasonable upper limit is 1MΩ. Normally R_G should not exceed this value.

Graphical Analysis

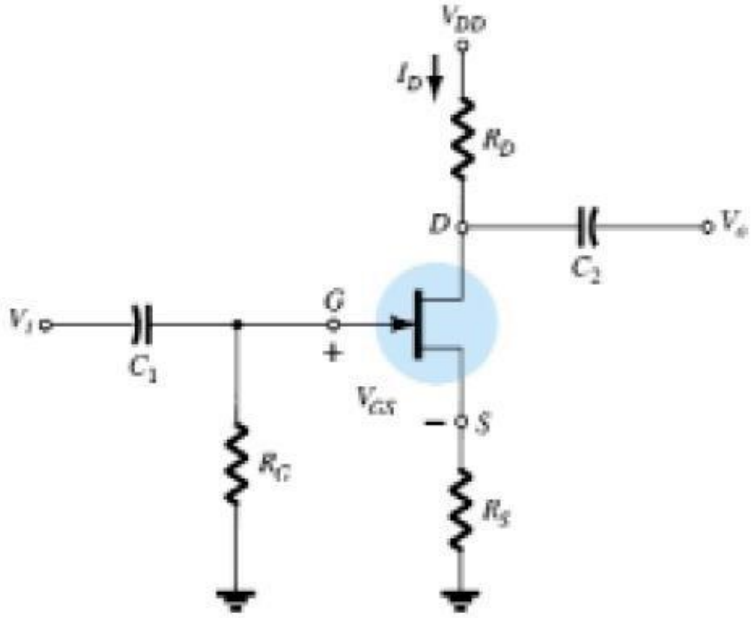
A graphical analysis would require a plot of Shockley's equation as shown in Fig. By choosing $I^{DSS}/4$ when plotting the equation. For the $V_{GS} = V_P/2$ will result in a drain current of analysis, the three points defined by I_{DSS} , V_P and the intersection just described will be sufficient for plotting the curve.



In Fig., the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$-the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration-commonly referred to as the quiescent or operating point. The subscript Q will be applied to drain current and gate-to-source voltage to identify their levels at the Q-point. Note in Fig. that the quiescent level of $I_D$is determined by drawing a horizontal line from the Q-point to the vertical $I_D$axis as shown in Fig.

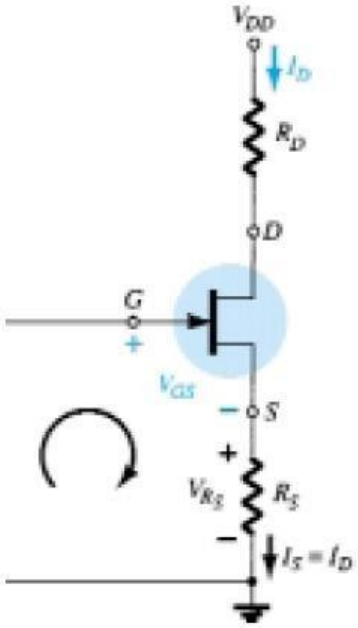


Self bias Configuration



- ✓ This is the most common method of biasing a JFET.
- ✓ This circuit eliminates the requirement of two dc supplies i.e. only drain supply is used and no gate supply is connected.
- ✓ In this circuit, a resistorR_S, known as bias resistor, is connected in the source lag.

The dc component of drain current I_D flowing through R_S makes a voltage drop acrossR_S. The voltage drop across R_S reduces the gate-to-source reverse voltage required for JFET operation. The resistorR_S, feedback resistor prevents any variation in drain current.



- ✓ since no gate current flows through the reverse bias gate-source, the gate current $I_G = 0$ and therefore, $V_G = I_G R_G = 0V$

- ✓ with the drain current I_D the voltage at source

$$V_S = I_D R_S = 0V$$

And the gate-source voltage V_{GS} is

$$V_{GS} = V_G - V_S = -I_D R_S$$

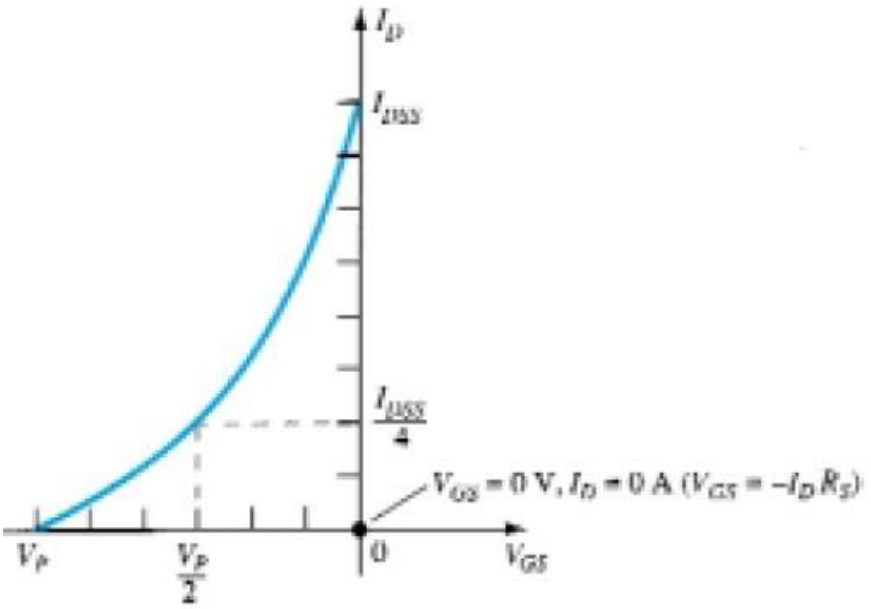
- ✓ So the voltage drop across the resistanceR_S, provides the biasing voltage V_{GS} and no external source is required for biasing, and this is the reason that it is called self biasing.
- ✓ The operating point (i.e. zero signal I_D and V_{DS}) can easily be determined by the equations

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Graphical Analysis

The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. Since Eq. $V_{GS} = -I_D R_S$ defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is $I_D = 0A$ since it results in $V_{GS} = -I_D R_S = 0V$. For Eq., therefore, one point on the straight line is defined by$I_D = 0A and\ V_{GS} = 0V$, as appearing on Fig.

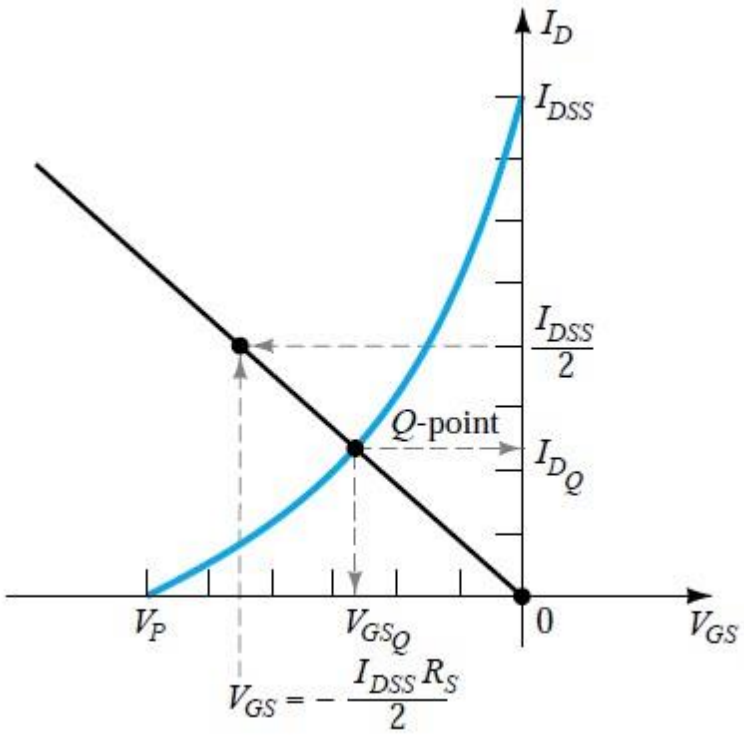


The second point for Eq. requires that a level of $V_{GS}\ or\ I_D$ be chosen and the corresponding level of the other quantity be determined using Eq. The resulting levels of $V_{GS}\ and\ I_D$will then define another point on the straight line and permit an actual drawing of the straight line. Suppose, for example, that we choose a level of $I_D$equal to one-half the saturation level. That is,

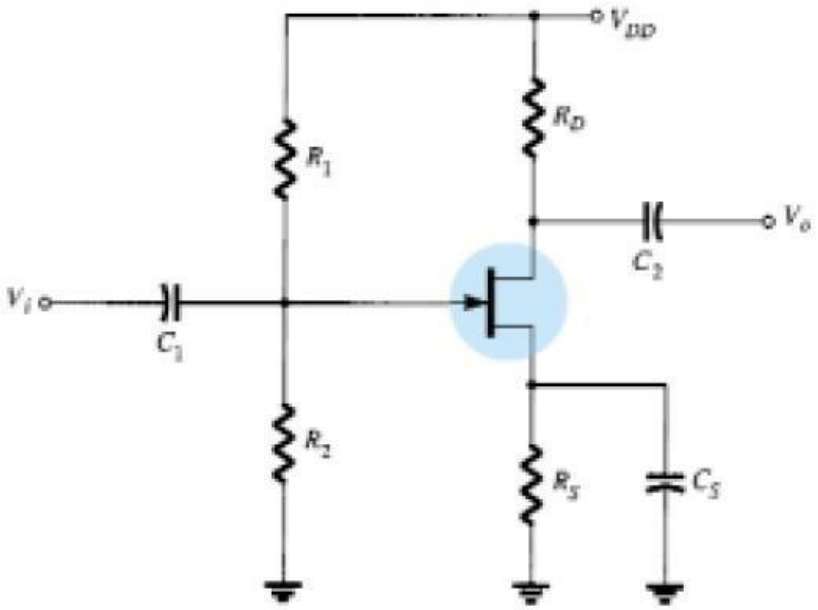
$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS}}{2} R_S$$

The result is a second point for the straight-line plot as shown in Fig. The straight line as defined by Eq. is then drawn and the quiescent point obtained at the intersection of the straight-line plot and the device characteristic curve. The quiescent values of $V_{GS}\ and\ I_D$can then be determined and used to find the other quantities of interest.

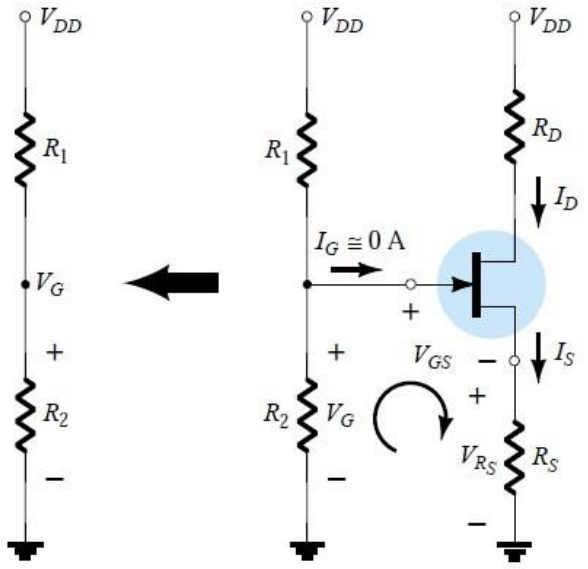


Voltage-divider bias Configuration



- ✓ The resistor R_1 and R_2 form a potential divider across the drain supplyV_{DD}.

- ✓ The voltage V_2 across R_2 provides necessary bias. The additional gate resistor R_1 form gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of large valuedR_S.



- ✓ The gate is reverse biased so that $I_G = 0$ and the gate voltage

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} R_2$$

And

$$V_{GS} = V_G - I_D R_S$$

- ✓ The circuit is so designed so that $I_D R_S$ is larger than V_G so that V_{GS} is negative. This provides correct bias voltage.

- ✓ The operating point can be determined as

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

- ✓ Maximum gain is achieved by making resistance R_D as large as possible and for a given level of I_D it needs maximum voltage drop across resistor R_D. However, greater bias stability is achieved by making R_S as large as possible.

Graphical Analysis

$$V_{GS} = V_G - I_D R_S$$

Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. the current $I_D = 0$. If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0mA$ into Eq. and finding the resulting value of V_{GS} as follows:

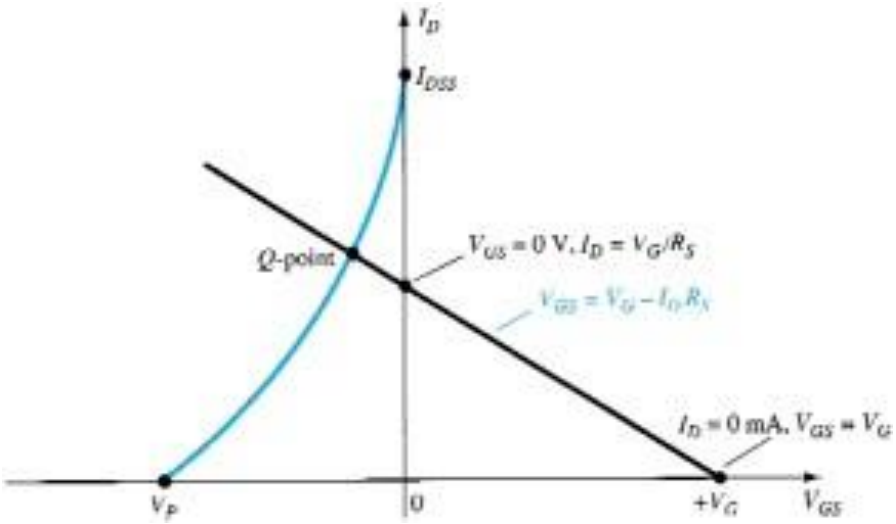
$$V_{GS} = V_G$$

The result specifies that whenever we plot Eq., if we choose $I_D = 0mA$, the value of for the plot V_{GS} will be V_G volts. The point just determined appears in Fig.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0V$ and solve for the resulting value of I_D:

$$I_D = \frac{V_G}{R_S}$$

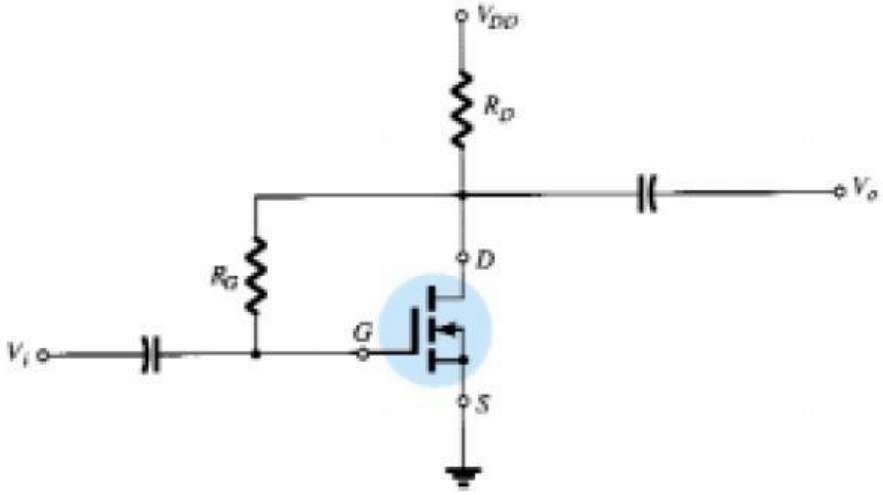
The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels ofI_D $and V_{GS}$.



Biasing of MOSFETs

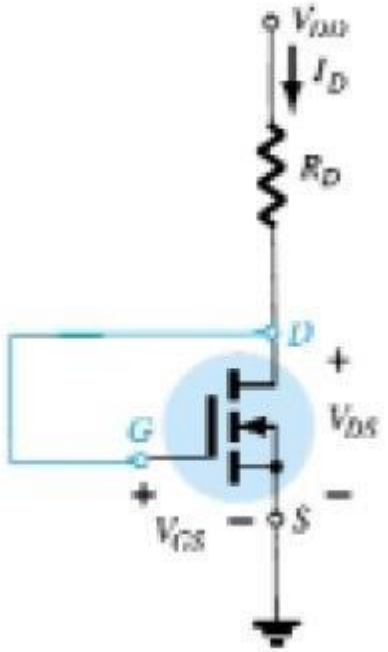
Feedback Biasing Arrangement

- ✓ A popular biasing arrangement for enhancement-type MOSFETs is provided in Figure.



- ✓ The resistor $R_G$brings a suitably large voltage to the gate to drive the MOSFET "on."

- ✓ Since $I_G = 0mA$ and$V_{RG} = 0V$, the dc equivalent network appears as shown in Fig.



✓ A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

$$V_{DS} = V_{GS}$$

✓ For the output circuit,

$$V_{DS} = V_{DD} — I_D R_D$$

which becomes

$$V_{GS} = V_{DD} — I_D R_D$$

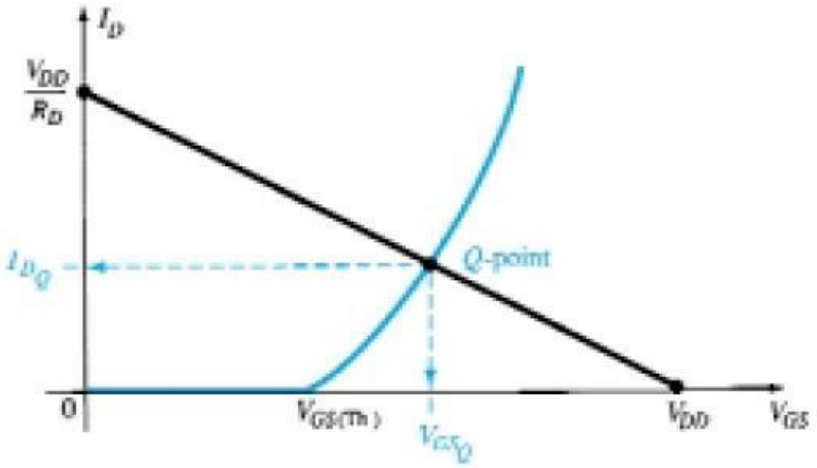
✓ Since the Eq. is that of a straight line, the procedure employed to determine the two points that will define the plot on the graph is as follows:
Substituting $I_D = 0mA$ into Eq. gives

$$V_{GS} = V_{DD} | I_D = 0mA$$

Substituting $V_{GS} = 0V$ into Eq.

$$I_D = \frac{V_{DD}}{R_D} \Big| V_{GS} = 0V$$

✓ The plots defined by the above Eqs. appear in Fig. with the resulting operating point.



Small Signal Analysis of BJTs

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Reference: 1. "Electronic Devices and Circuit Theory"

Robert L. Boylestad and L. Nashelsky

2. "Microelectronics Circuits"

Sedra and Smith

Small Signal Operation-BJTs

Introduction

There are three models commonly used in the small signal ac analysis of transistor networks:

- ✓ The r_e model
- ✓ The hybrid-π model
- ✓ The hybrid equivalent model

BJT Transistor modelling

The key to transistor small-signal analysis is the use of the equivalent circuits (models). **A MODEL IS A COMBINATION OF CIRCUIT ELEMENTS LIKE VOLTAGE OR CURRENT SOURCES, RESISTORS, CAPACITORS** etc, that best approximates the behavior of a device under specific operating conditions. Once the model (ac equivalent circuit) is determined, the schematic symbol for the device can be replaced by the equivalent circuit and the basic methods of circuit analysis applied to determine the desired quantities of the network.

Hybrid equivalent network: employed initially. It is defined for a set of operating conditions that might not match the actual operating conditions.

r_e model: desirable, but does not include feedback term

Hybrid-π model: model of choice.

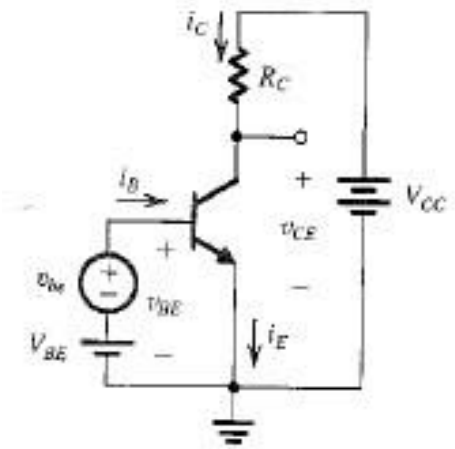
AC equivalent of a network

AC equivalent of a network is obtained by:

- ✓ Setting all dc sources to zero and replacing them by a short-circuit equivalent
- ✓ Replacing all capacitors by short-circuit equivalent
- ✓ Removing all elements bypassed by the short-circuit equivalent.
- ✓ Redrawing the network in a more convenient and logical form.

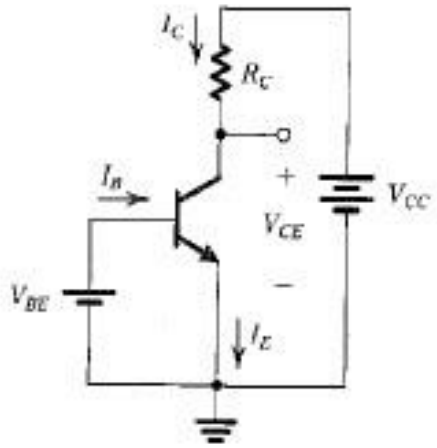
Small-Signal Operation and Models

Consider the circuit shown in the Fig.



Here the base-emitter junction is forward biased by a dc voltage V_{BE}(battery). The reverse bias of the collector-base junction is established by connecting the collector to another power supply of voltage V_{CC}through a resistorR_C. The input signal to be amplified is represented by the voltage source v_{be} that is superimposed onV_{BE}.

We consider first the dc bias conditions by setting the signal v_{be} to zero. The circuit reduces to that in Fig. and then write the following relationships for the dc currents and voltages.



$$I_C = I_S e^{V_{BE}/V_T}$$

$$I_E = I^C/\alpha$$

$$I_B = Ic/\beta$$

$$V_C = V_{CE} = V_{CE} - I_C R_C$$

The Collector Current and the Transconductance

If a signal v_{be} is applied as shown in Fig, the total instantaneous base-emitter voltage v_{BE}becomes

$$v_{BE} = V_{BE} + v_{be}$$

Correspondingly, the collector current becomes

$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T}$$

$$= I_S e^{v_{BE}/V_T} e^{v_{be}/V_T}$$

$$= I_C e^{v_{be}/V_T}$$

Now, if $v_{be} \ll V_T$, we may write

$$i_C \cong I_C(1 + \frac{v_{be}}{V_T})$$

This approximation is valid for only v_{be}less than approximately 10mV, is referred as the small-signal approximation.

$$i_C = I_C + I_C \frac{v_{be}}{V_T}$$

Thus, the collector current is composed of the dc bias value I_C and a signal componenti_c

$$i_c = I_C \frac{v_{be}}{V_T}$$

This equation relates the signal current in the collector to the corresponding base-emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be}$$

Where $g_m$is called the transconductance and it is given by

$$g_m = \frac{I_C}{V_T}$$

The Base Current and the Input Resistance at the Base

To determine the resistance seen by v_{be}, we first evaluate the total base current i_B

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T}v_{be}$$

Thus, $i_B = I_B + i_b$

The signal component $i_b$is given by

$$i_b = \frac{1}{\beta}\frac{I_C}{V_T}v_{be}$$

Substituting

$I^C/V_T$by $g_m$gives

$$i_b = \frac{g_m}{\beta}v_{be}$$

The small signal input resistance between base and emitter, looking in to the base, is denoted by $r_\pi$and is defined as

$$r_\pi \equiv \frac{v_{be}}{i_b}$$

Or,

$$r_\pi \equiv \frac{\beta}{g_m}$$

Or,

$$r_\pi \equiv \frac{V_T}{I_B}$$

The Emitter Current and the Input Resistance at the Emitter

The total emitter current i_E can be determined from

$$i_E = \frac{i_C}{\alpha} = \frac{\mathrm{I}_C}{\alpha} + \frac{i_c}{\alpha}$$

Thus, $$i_E = I_E + i_e$$

The signal current i_e is given by,

$$i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be}$$

We denote the small-signal resistance between base and emitter, looking into the emitter, by r_e and can be defined as

$$r_e \equiv \frac{v_{be}}{i_e}$$

We find that r_e called emitter resistance, is given by

$$r_e = \frac{V_T}{I_E}$$

Or $$r_e = \frac{\alpha}{g_m} \approx \frac{1}{g_m}$$

Relationship between $r_\pi$and r_e

$$v_{be} = i_b r_\pi = i_e r_e$$

$$r_\pi = (i_e / i_b) r_e$$

Which yields,

$$r_\pi = (\beta + 1) r_e$$

Separating the Signal and the DC Quantities

The analysis above indicates that every current and voltage in the amplifier circuit of is composed of two components: a dc component and a signal component. For instance, $v_{BE} = V_{BE} + v_{be}$, $i_C = I_C + i_c$ and so on. The dc components are determined from the dc circuit and from the relationships imposed by the transistor. On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources, as shown in Fig. Observe that since the voltage of an ideal dc supply does not change, the signal voltage across it will be zero. For this reason we have replaced V_{CC} and V_{BE} with short circuits. Had the circuit contained ideal dc current sources, these would have been replaced by open circuits. Note, however, that the circuit of Fig. is useful only in so far as it shows the various signal currents and voltages; it is not an actual amplifier circuit since the dc bias circuit is not shown.

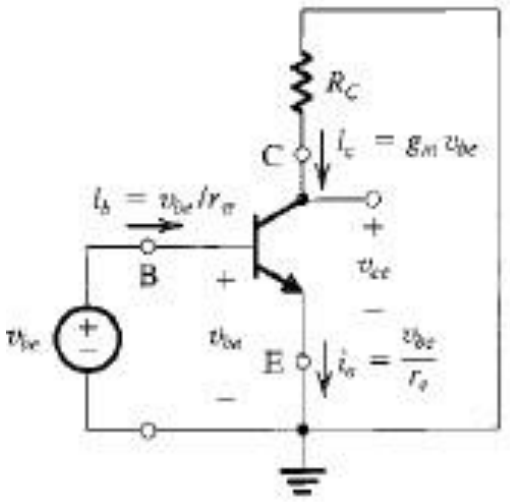
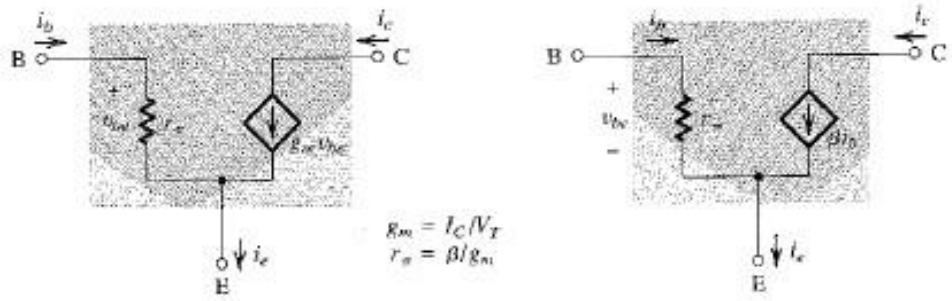


Figure also shows the expressions for the current increments *(i_c,i_e,* and *i_b)* obtained when a small signal v_{be} is applied. These relationships can be represented by a circuit. Such a circuit should have three terminals-C, B, and E and should yield the same terminal currents indicated in Fig. The resulting circuit is then equivalent to the transistor as far as small-signal operation is concerned, and thus it can be considered an equivalent small-signal circuit model.

The Hybrid-π Model

An equivalent circuit model for the BJT is shown in Fig. (a) represents BJT as a voltagecontrolled current source (a transconductance amplifier), and (b) represents BJT as a current-controlled current source (a current amplifier)



(a) (b)

The r_e Transistor Model

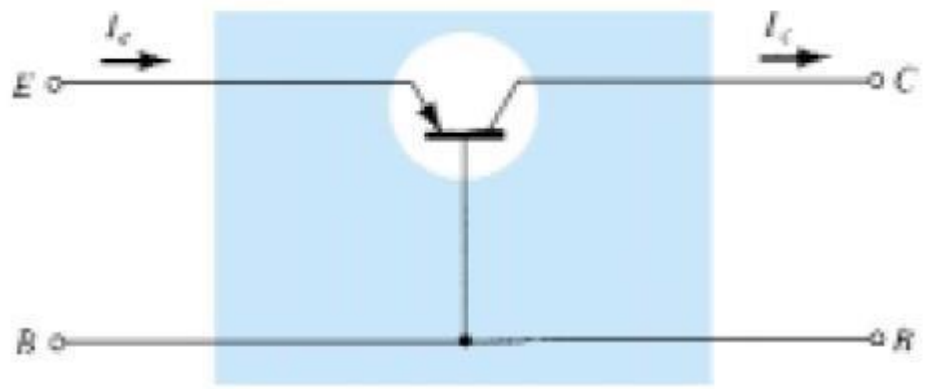
- ✓ The r_e model employs a diode and controlled current source to duplicate the behaviour of a transistor.

- ✓ A current-controlled current source is one where the parameters of the current source are controlled by a current elsewhere in the network.

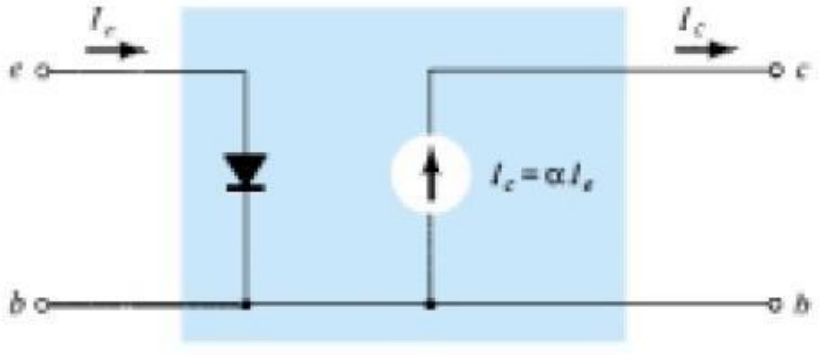
- ✓ In general, BJT transistor amplifiers are referred to as current-controlled devices.

Common Base Configuration

- ✓ In Fig., a common-base pnp transistor has been inserted within the two-port structure.



- ✓ The r_e model for the transistor has been placed between the same four terminals as shown in Fig.



- ✓ The results obtained with the model in place should be relatively close to those obtained with the actual transistor.

- ✓ The forward-biased junction will behave much like a diode (ignoring the effects of changing levels ofV_{CE}).

- ✓ For the output side, the horizontal curves revealed that $I_c \cong I_e$ (as derived from$I_c = \alpha I_e$) for the range of values ofV_{CE}.

- ✓ The current source establishes the fact that $I_c = \alpha I_e$, with the controlling current I_e appearing in the input side of the equivalent circuit.

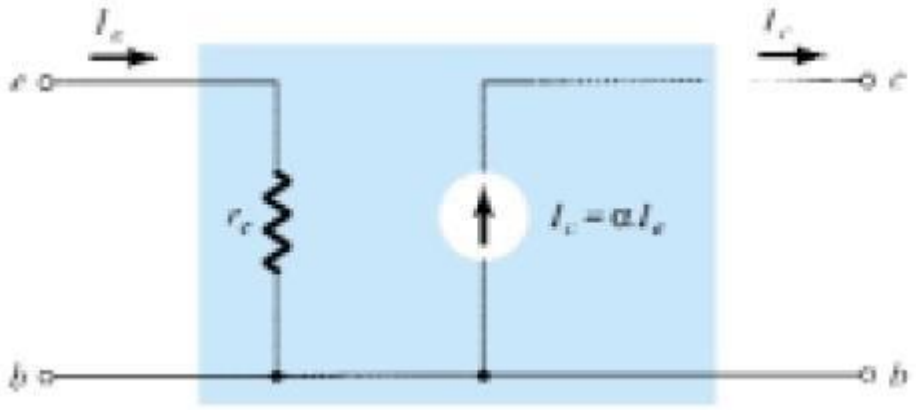
- ✓ The ac resistance of a diode can be determined by the equation

$$r_{ac} = \frac{26\text{mV}}{I_D}$$

where $I_D$is the dc current through the diode at the Q (quiescent) point.

- ✓ This same equation can be used to find the ac resistance of the diode of Fig. if we simply substitute the emitter current as follows

$$r_e = \frac{26\text{mV}}{I_E}$$



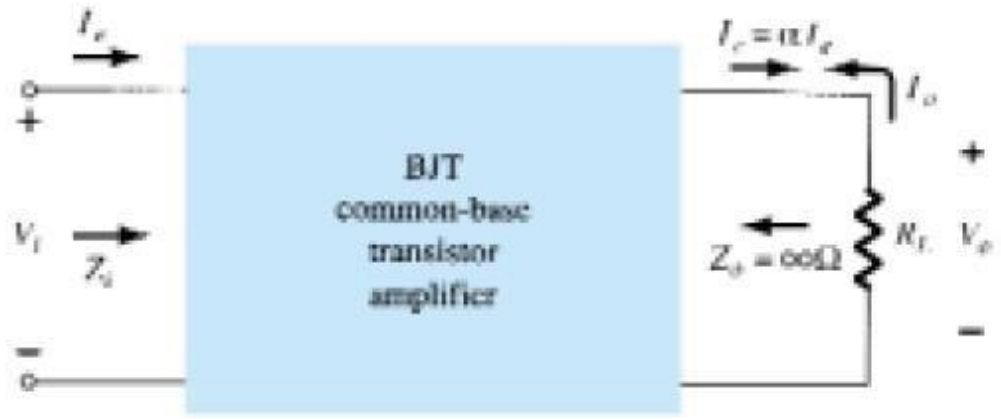
- ✓ The input impedance Z_i for the common-base configuration of a transistor is simplyr_e. Typical values of Z_i range from a few ohms to a maximum of about 50 Ω.

$$Z_i = r_e$$

- ✓ For the output impedance, if we set the signal to zero, then $I_e = 0\ A$ and $I_c = \propto I_e = 0A$, resulting in an open-circuit equivalence at the output terminals. The result is that for the model of Fig.

✓ For the common-base configuration, typical values of $Z_0$are in the mega ohm range.

✓ The voltage gain will now be determined for the network of Fig.



$$V_0 = -I_0 R_L = -(-I_C R_L) = \alpha I_e R_L$$

$$and\ V_i = I_e Z_i = I_e r_e$$

$$A_V = \frac{V_0}{V_i} = \frac{\alpha I_e R_L}{I_e r_e}$$

$$A_V = \frac{\alpha R_L}{r_e} \cong \frac{R_L}{r_e}$$

✓ For current gain

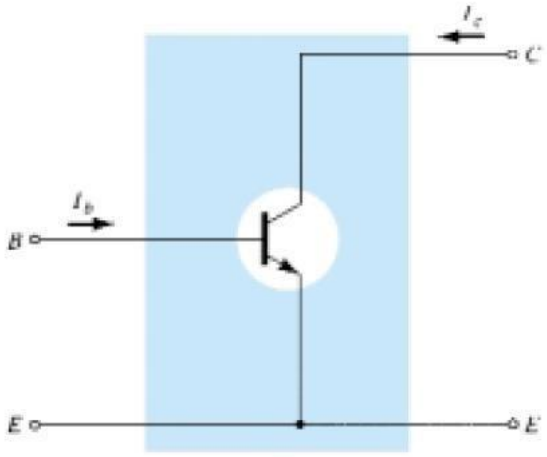
$$A_i = \frac{I_0}{I_i} = \frac{-I_C}{I_e} = \frac{-\alpha I_e}{I_e}$$

$$A_i = -\alpha = -1$$

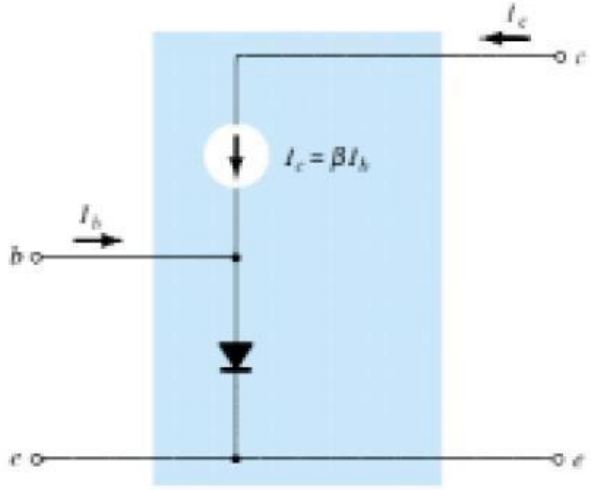
Common Emitter Configuration

- ✓ For the common-emitter configuration of Fig., the input terminals are the base and emitter terminals, but the output set is now the collector and emitter terminals.

- ✓ The emitter terminal is now common between the input and output ports of the amplifier.



- ✓ Substituting the $r_e$equivalent circuit for the *npn* transistor will result in the configuration of Fig.



- ✓ The controlled-current source is connected between the collector and base terminals and the diode between the base and emitter terminals.

- ✓ The base current is the input current while the output current isI_c.

$$I_c = \beta I_b$$

- ✓ The current through the diode is therefore determined by

$$I_e = I_b + I_c = I_b + \beta I_b$$

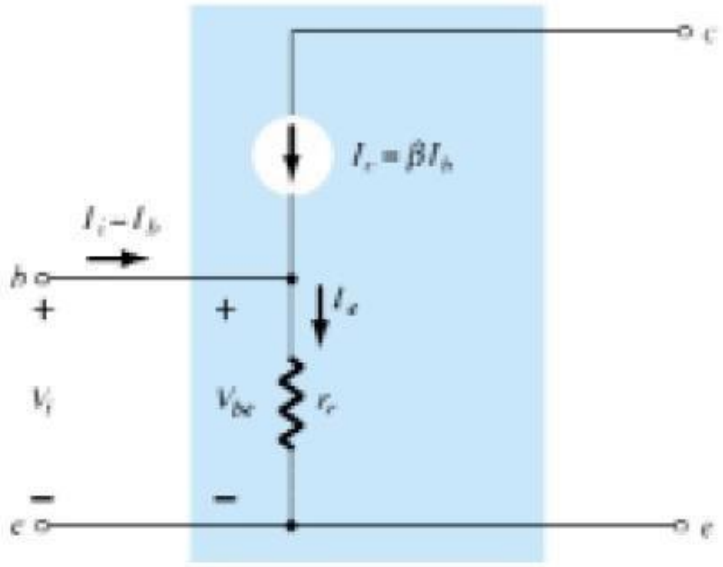
$$I_e = (\beta + 1) I_b$$

$$I_e \cong \beta I_b$$

- ✓ The input impedance is determined by the following

$$Z_i = \frac{V_i}{I_i} = \frac{V_{be}}{I_b}$$

- ✓ The voltage $V_{be}$is across the diode resistance as shown in Fig.



- ✓ The level of $r_e$is still determined by the dc currentI_E. Using Ohm's law gives

$$V_i = V_{be} = I_e r_e \cong \beta I_b r_e$$

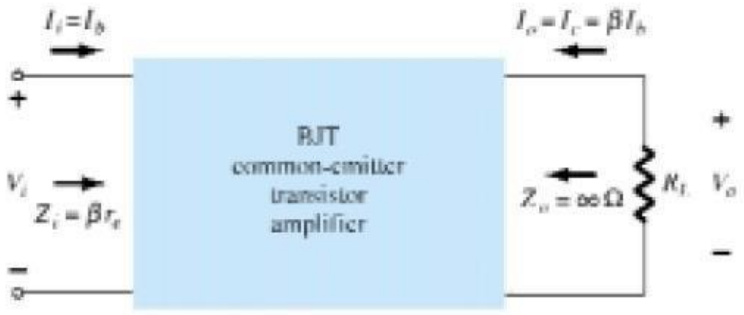
$$Z_i = \frac{V_{be}}{I_b} \cong \frac{\beta I_b r_e}{I_b}$$

$$Z_i \cong \beta r_e$$

- ✓ For the common-emitter configuration, typical values of Z_i defined by βr_e range from a few hundred ohms to the kilo ohms range, with maximums of about 6–7 kΩ.

- ✓ The output impedance is $Z_0 = r_0$ and the typical values of Z_0 are in the range of40 to 50 kΩ.

- ✓ The voltage gain for the common-emitter configuration will now be determined for the configuration of Fig. using the assumption that $Z_0 = \infty\Omega$.



- ✓ The output voltage

$$V_0 = -I_0 R_L = -I_c R_L = -\beta I_b R_L$$

$$and\ V_i = I_i Z_i = \beta I_b r_e$$

$$so\ that\ A_V = \frac{V_0}{V_i} = -\frac{\beta I_b R_L}{\beta I_b r_e}$$

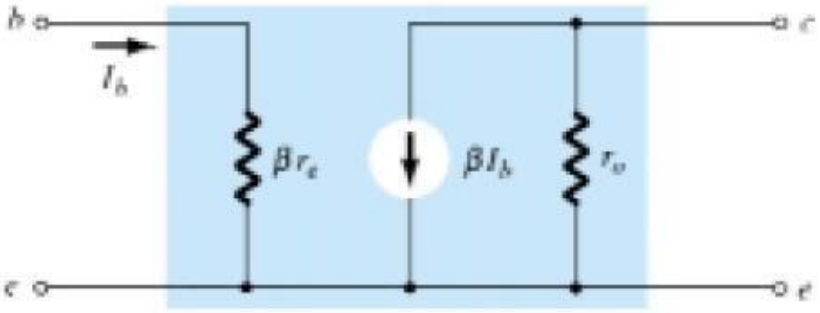
$$and\ \boxed{A_V = -\frac{R_L}{r_e}}$$

- ✓ The current gain for the configuration

$$A_i = \frac{I_0}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$$

$$\boxed{A_i = \beta}$$

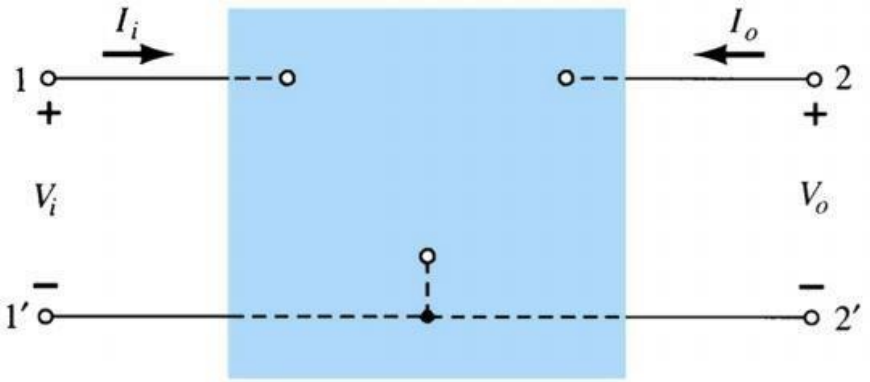
- ✓ Using the input impedance βr_e , the collector current βI_b , and the output impedancer_0, the equivalent model is shown in figure.



- ✓ For typical parameter values, the common-emitter configuration can be considered one that has a moderate level of input impedance, a high voltage and current gain, and output impedance that may have to be included in the network analysis.

The Hybrid equivalent model

- ✓ For the hybrid equivalent model, the parameters are defined at an operating point.
- ✓ The quantitiesh_{ie}, h_{re}, h_{fe}, and h_{oe}, are called hybrid parameters and are the components of a small-signal equivalent circuit.
- ✓ The description of the hybrid equivalent model will begin with the general two port system.



The set of equations in which the four variables can be related are:

$$V_i = h_{11}I_i + h_{12}V_0$$

$$I_0 = h_{21}I_i + h_{22}V_0$$

- ✓ The four variables h_{11}, h_{12}, h_{21}, and h_{22}, are called hybrid parameters (the mixture of variables in each equation results in a " hybrid" set of units of measurement for the h-parameters.
- ✓ Set $V_0 = 0$, solving for h_{11}, $h_{11} = {}^{V_i}/_{I_i}\, ohms$
  This is the ratio of input voltage to the input current with the output terminals shorted. It is called Short circuit input impedance parameter.

- ✓ If I_i is set equal to zero by opening the input leads, we get expression for h_{12}

  h_{12} = V^i/V_0, This is called open circuit reverse voltage ratio.

- ✓ Again by setting $V_0 = 0$ and shorting the output terminals, we get $h_{21} =$

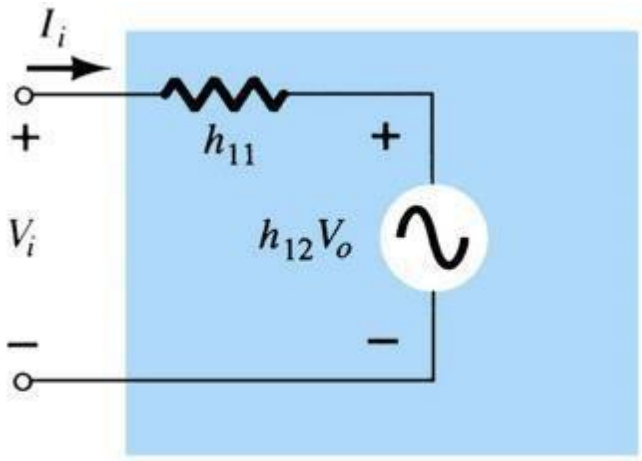
  ${}^{I_0}/_{I_i}$known as short circuit forward transfer current ratio.

- ✓ Again by setting $I_i = 0$ and by opening the input leads$h_{22} = {}^{I_0}/_{V_0}$, this is known

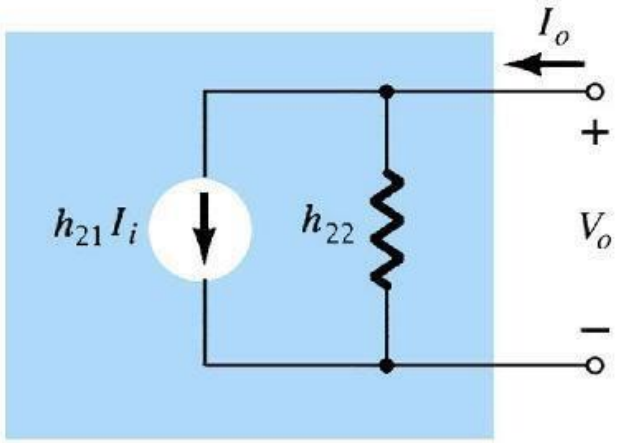
  as open circuit output admittance. This is represented as resistor ($1/h_{22}$)

$h_{11} = h_i$= input resistance $h_{12} = h_r$= reverse transfer voltage ratio $h_{21} = h_f$= forward transfer current ratio $h_{22} = h_0$= Output conductance

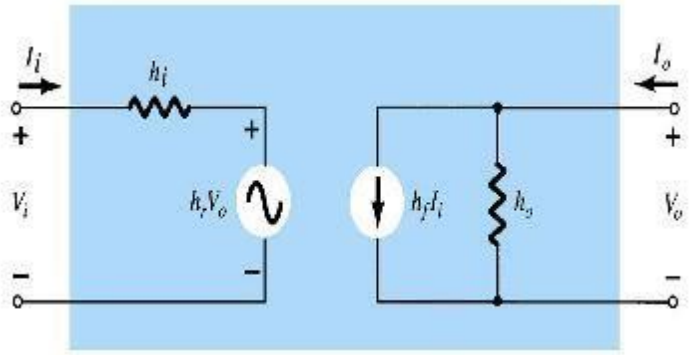
Hybrid Input equivalent circuit



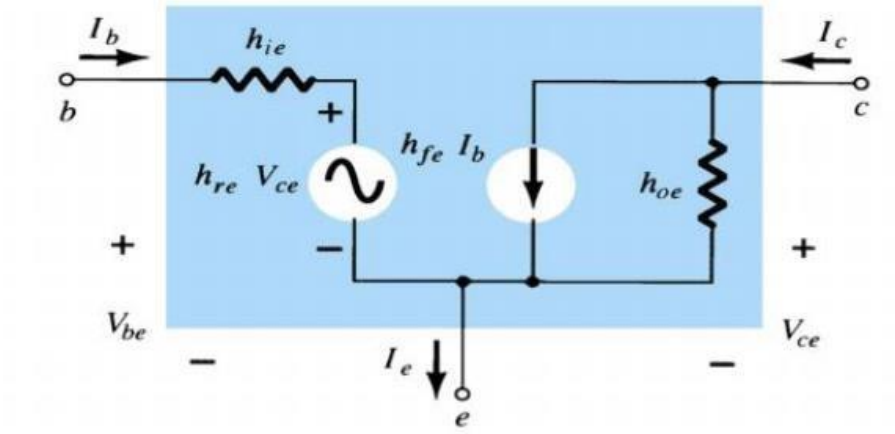
Hybrid output equivalent circuit



Complete hybrid equivalent circuit

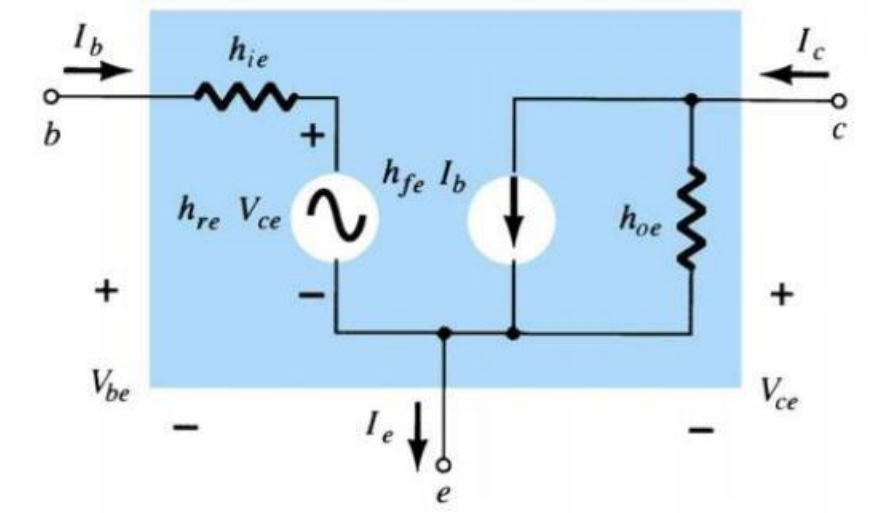


Common Emitter Configuration - hybrid equivalent circuit



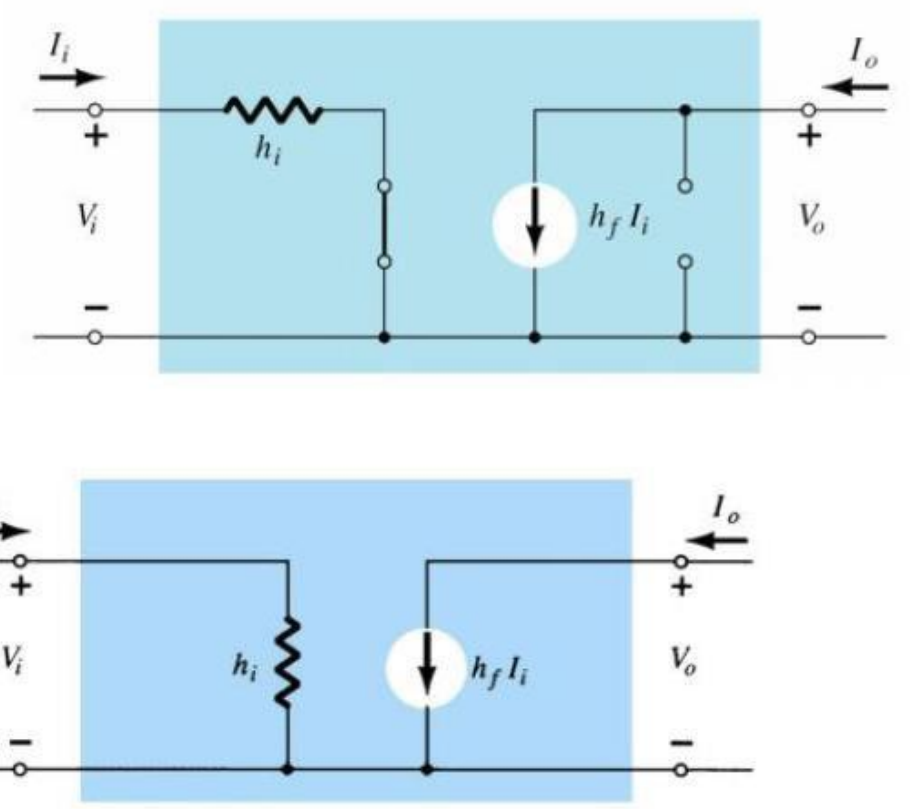
- ✓ Essentially, the transistor model is a three terminal two-port system.
- ✓ The h-parameters, however, will change with each configuration.
- ✓ To distinguish which parameter has been used or which is available, a second subscript has been added to the h – parameter notation.
- ✓ For the common-base configuration, the lowercase letter b is added, and for common emitter and common collector configurations, the letters e and c are used respectively.

Common Base configuration - hybrid equivalent circuit



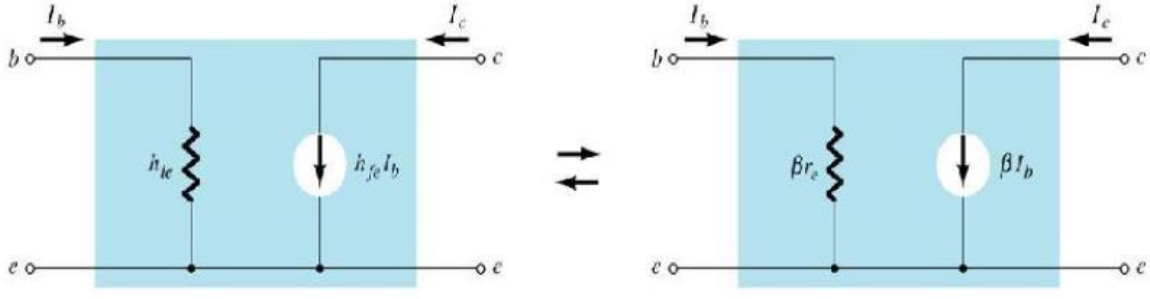
- ✓ Normally h_r is a relatively small quantity, its removal is approximated by $h_r \cong 0$ and $h_r V_o = 0$, resulting in a short-circuit equivalent.

- ✓ The resistance determined by $1/h_o$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open-circuit equivalent.



h- Parameter Model v/s. r_e Model

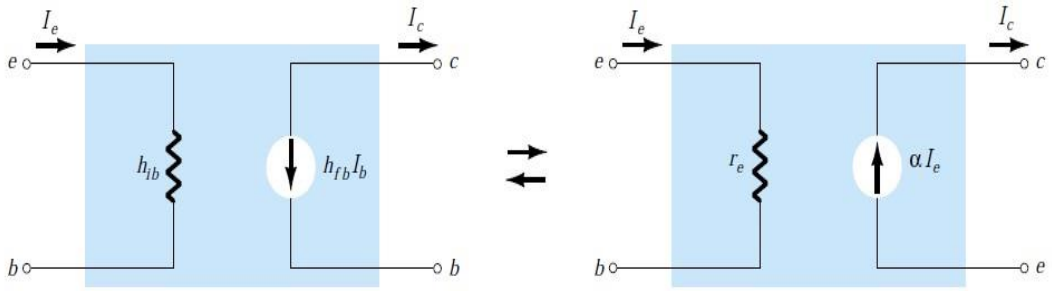
Common-emitter configuration



$$h_{ie} = \beta r_e$$

$$h_{fe} = \beta_{ac}$$

Common-base configuration



$$h_{ib} = r_e$$

$$h_{fb} = -\alpha \cong -1$$

Graphical Determination of h-parameters

- ✓ Using partial derivatives (calculus), it can be shown that the magnitude of the h-parameters for the small-signal transistor equivalent circuit in the region of operation for the common-emitter configuration can be found using the following equations:

$$h_{ie} = \frac{\partial v_i}{\partial i_i} = \frac{\partial v_{be}}{\partial i_b} \cong \frac{\Delta v_{be}}{\Delta i_b} | V_{CE} = constant$$

$$h_{re} = \frac{\partial v_i}{\partial v_0} = \frac{\partial v_{be}}{\partial v_{ce}} \cong \frac{\Delta v_{be}}{\Delta v_{ce}} | I_B = constant$$

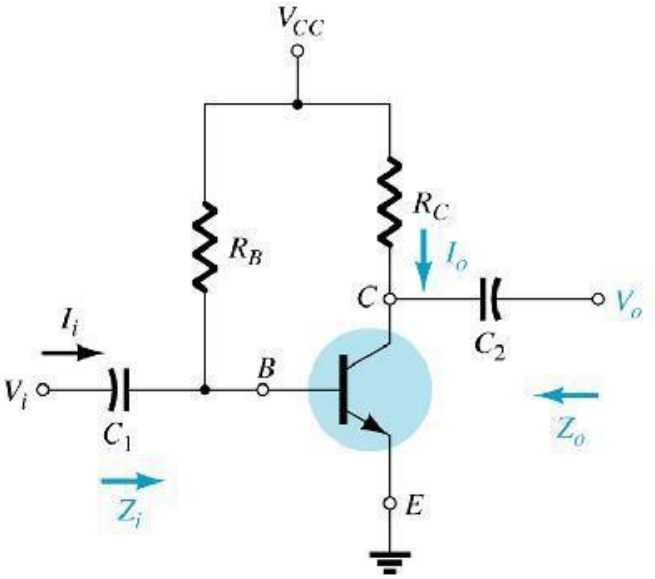
$$h_{fe} = \frac{\partial i_0}{\partial i_i} = \frac{\partial i_c}{\partial i_b} \cong \frac{\Delta i_c}{\Delta i_b} | V_{CE} = constant$$

$$h_{oe} = \frac{\partial i_0}{\partial v_0} = \frac{\partial i_c}{\partial v_{ce}} \cong \frac{\Delta i_c}{\Delta v_{ce}} | I_B = constant$$

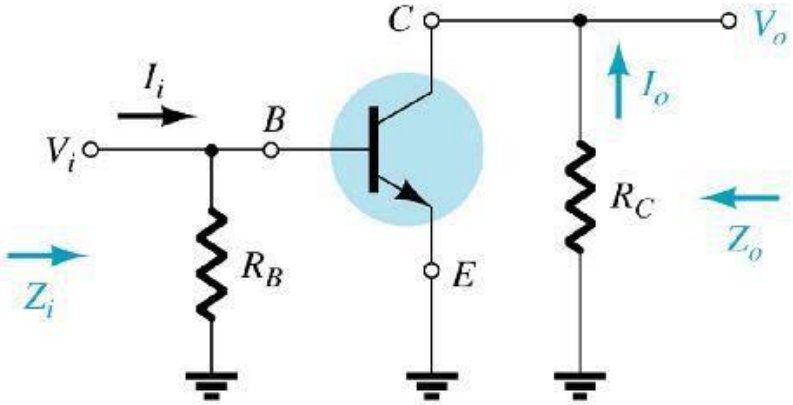
Note that the partial derivative $\frac{\partial v_i}{\partial i_i}$ provides a measure of the instantaneous change in $v_i$due to an instantaneous change inI_i.

- ✓ In each case, the symbol Δ refers to a small change in that quantity around the quiescent point of operation.
- ✓ In other words, the *h*-parameters are determined in the region of operation for the applied signal so that the equivalent circuit will be the most accurate available.
- ✓ The constant values of $V_{CE}$and $I_B$in each case refer to a condition that must be met when the various parameters are determined from the characteristics of the transistor.
- ✓ For the common-base and common-collector configurations, the proper equation can be obtained by simply substituting the proper values ofv_i, v_0, i_i, andi_0.
- ✓ The parameters h_{ie} and h_{re} are determined from the input or base characteristics, while the parameters $h_{fe}$and $h_{oe}$are obtained from the output or collector characteristics.

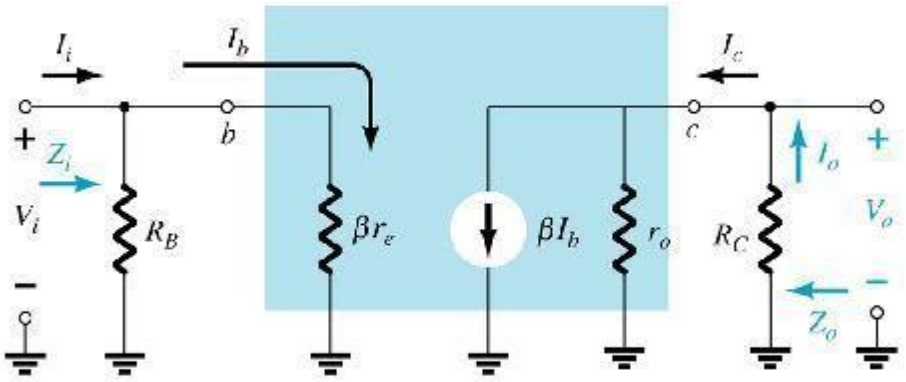
Common Emitter - Fixed bias configuration



Removing DC effects of V_{CC} and Capacitors



r_e Model



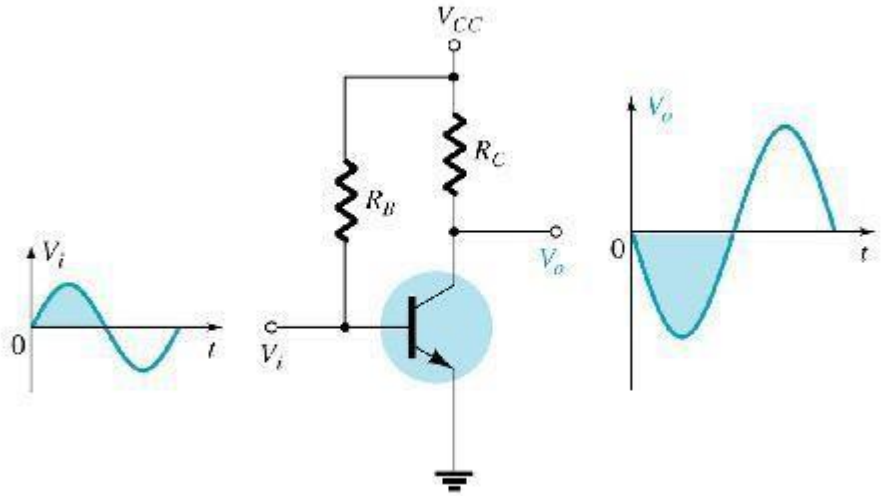
Small signal analysis – fixed bias

$r_e$model	Hybrid model	Hybrid-π model
Input Impedance $Z_i = R_B \parallel \beta r_e$ If $R_B \geq 10\beta r_e$, then $R_B \parallel \beta r_e \cong \beta r_e$ $\boxed{Z_i \cong \beta r_e}$	**Input Impedance** $Z_i = R_B \parallel h_{ie}$ $R_B \parallel h_{ie} \cong h_{ie}$ $\boxed{Z_i \cong h_{ie}}$	**Input Impedance** $Z_i = R_B \parallel r_\pi$ $R_B \parallel r_\pi \cong r_\pi$ $\boxed{Z_i \cong r_\pi}$
Output Impedance Z_0 is the output impedance when$V_i = 0$. When $V_i = 0$, $i_b = 0$, resulting in open circuit equivalence for the current source. $\boxed{Z_0 = R_C \parallel r_o}$	**Output Impedance** Z_0 is the output impedance when $V_i = 0$. When $V_i = 0, i_b = 0$, resulting in open circuit equivalence for the current source. $\boxed{Z_0 = R_C \parallel 1/h_{0e}}$	**Output Impedance** Z_0 is the output impedance when $V_i = 0$. When $V_i = 0, i_b = 0$, resulting in open circuit equivalence for the current source. $\boxed{Z_0 = R_C \parallel r_o}$
Voltage gain A_V	**Voltage gain A_V**	**Voltage gain A_V**

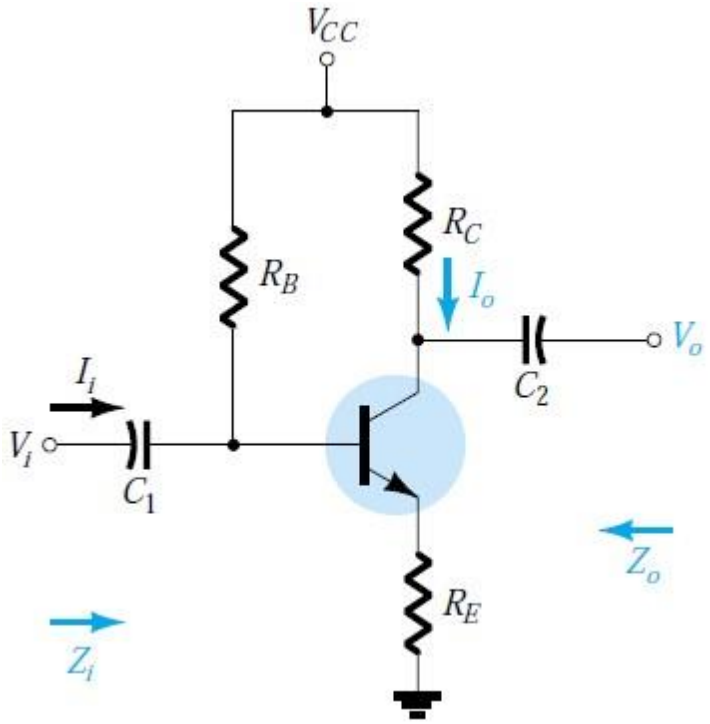
$V_0 = -\beta I_b(R_C \parallel r_0)$ From r_e model, $I_b = \frac{V_i}{\beta r_e}$ $V_0 = -\beta \frac{V_i}{\beta r_e}(R_C \parallel r_0)$ $A_V = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_0)}{r_e}$ If $r_0 \geq 10R_C$ $A_V = -\frac{R_C}{r_e}$	$V_0 = -h_{fe}I_b(R_C \parallel 1/h_{0e})$ From hybrid model, $I_b = \frac{V_i}{h_{ie}}$ $V_0 = -h_{fe}\frac{V_i}{h_{ie}}(R_C \parallel 1/h_{0e})$ $A_V = \frac{V_o}{V_i} = -h_{fe}\frac{(R_C \parallel 1/h_{0e})}{h_{ie}}$	$V_0 = -g_m V_\pi(R_C \parallel r_0)$ From hybrid-π model, $V_i = V_\pi = V_{be}$ $V_0 = -g_m V_i(R_C \parallel r_0)$ $A_V = \frac{V_o}{V_i} = -g_m(R_C \parallel r_o)$

Phase Shift

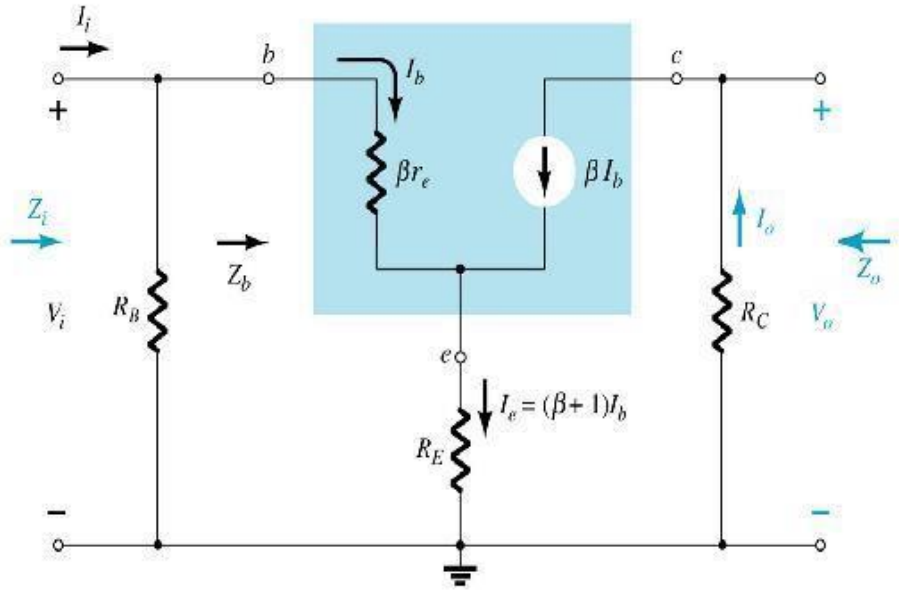
The negative sign in the gain expression indicates that there exists 180°phase shift between the input and output.



Common Emitter – Unbypassed Emitter bias configuration



Equivalent Circuit



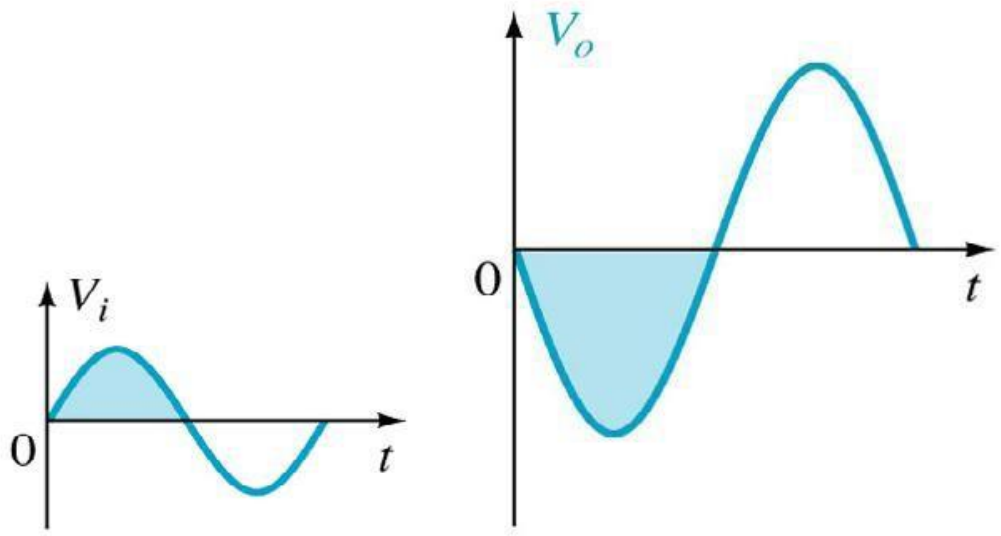
$r_e$model	Hybrid model	Hybrid-π model

Input Impedance Applying KVL to the input side: $V_i = I_b\beta r_e + I_eR_E$ $V_i = I_b\beta r_e + (\beta + 1)I_bR_E$ Input impedance looking into the network to the right of R_B is $Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$ + = $Z_b = \frac{V_i}{I_b} = \beta(r_e + R_E)$ Since $\beta \gg 1$ $(\beta \quad 1) \quad \beta$ Since R_E is often much greater than r_e $Z_b = \beta r_e$ $Z_i = R_B \parallel Z_b$	**Input Impedance** Applying KVL to the input side: $V_i = I_bh_{ie} + I_eR_E$ $V_i = I_bh_{ie} + (h_{fe} + 1)I_bR_E$ Input impedance looking into the network to the right of R_B is $Z_b = \frac{V_i}{I_b} = h_{ie} + h_{fe}R_E$ Since $h_{fe} \gg h_{ie}$ $Z_b \cong h_{fe}R_E$ $Z_i = R_B \parallel Z_b$	**Input Impedance** Applying KVL to the input side: $V_i = I_br_\pi + I_eR_E$ $V_i = I_br_\pi + (\beta + 1)I_bR_E$ Input impedance looking into the network to the right of R_B is $Z_b = \frac{V_i}{I_b} = r_\pi + (1 + \beta)R_E$ $Z_i = R_B \parallel Z_b$
Output Impedance Z_o is determined by setting V_i to zero, $I_b = 0$ and βI_b can be replaced by open circuit equivalent. $Z_0 = R_C$	**Output Impedance** $Z_0 = R_C$	**Output Impedance** $Z_0 = R_C$
Voltage gain A_V $V_o = -I_0R_C$ $V_o = -\beta I_bR_C$ $= -\beta \frac{V_i}{Z_b} R_C$	**Voltage gain A_V** $V_o = -I_0R_C$ $V_o = -h_{fe}I_bR_C$ $= -h_{fe} \frac{V_i}{Z_b} R_C$	**Voltage gain A_V** $V_o = -I_0R_C$ $V_o = -\beta I_bR_C$ $= -\beta \frac{V_i}{Z_b} R_C$

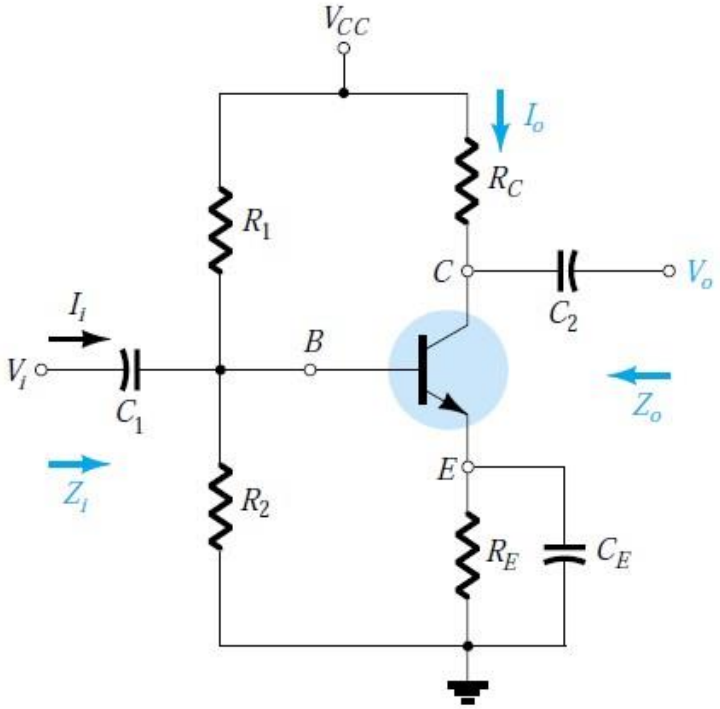
$A_V = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}$ Substituting, $Z_b = \beta(r_e + R_E)$ $A_V = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E}$ $R_E \gg r_e$, $A_V = -\frac{R_C}{R_E}$	$A_V = \frac{V_o}{V_i} = -\frac{h_{fe} R_C}{Z_b}$ Substituting, $Z_b \cong h_{fe} R_E$ $A_V = -\frac{R_C}{R_E}$	$A_V = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}$ Substituting, $Z_b = r_\pi + (1+\beta)R_E$ $A_V = -\frac{\beta R_C}{r_\pi + (1+\beta)R_E}$ $(1+\beta)R_E \gg r_\pi$ $A_V = -\frac{R_C}{R_E}$

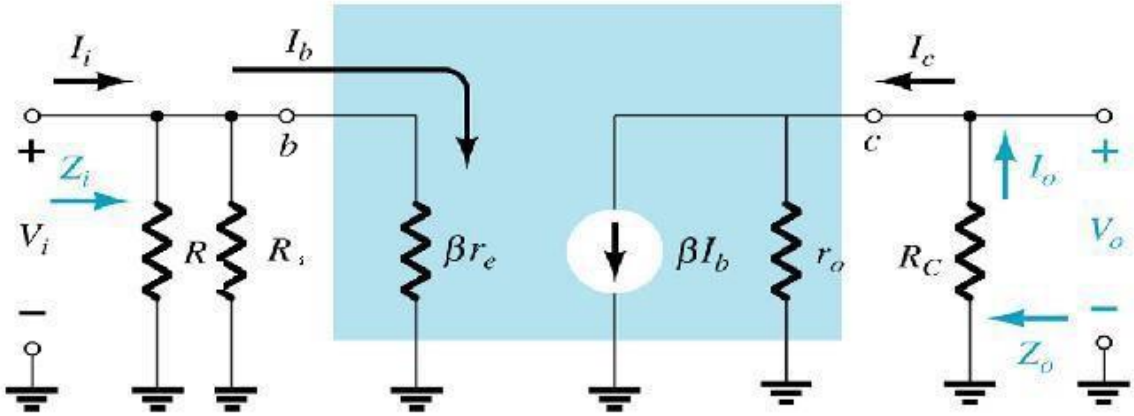
Phase Shift

The negative sign in the gain equation reveals a 180°phase shift between input and output.



Common Emitter – Voltage divider bias configuration





- ✓ The re model is very similar to the fixed bias circuit except for R_B is $R_1 \parallel R_2$in the case of voltage divider bias.

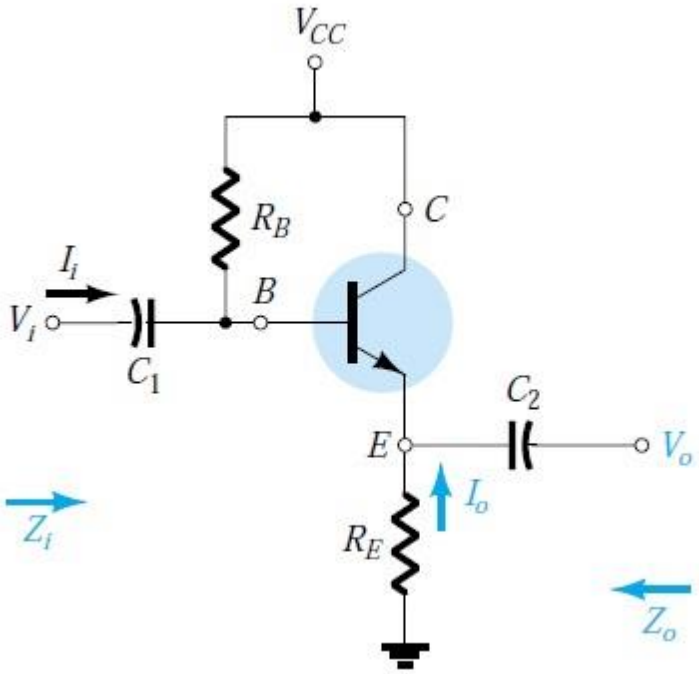
- ✓ Expression for A_V remains the same.

Small signal analysis – voltage divider bias

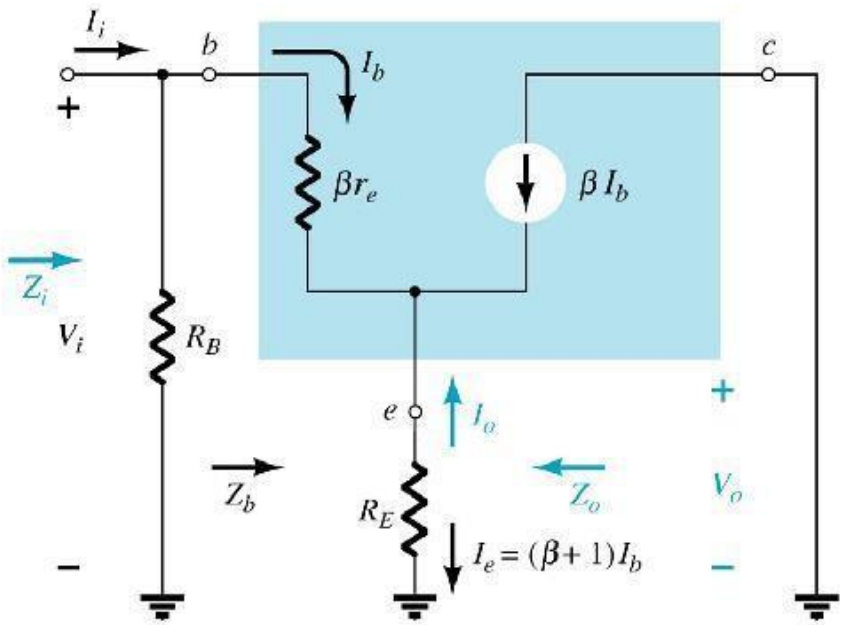
$r_e$model	Hybrid model	Hybrid-π model
Input Impedance $Z_i = R' \parallel \beta r_e$ Where $R' = R_1 \parallel R_2$	**Input Impedance** $Z_i = R' \parallel h_{ie}$ Where $R' = R_1 \parallel R_2$	**Input Impedance** $Z_i = R' \parallel r_\pi$ Where $R' = R_1 \parallel R_2$
Output Impedance Z_0 is the output impedance when $V_i = 0$. When $V_i = 0$, $i_b = 0$, resulting in open circuit equivalence for the current source. $Z_0 = R_C \parallel r_o$	**Output Impedance** Z_0 is the output impedance when $V_i = 0$. When $V_i = 0, i_b = 0$, resulting in open circuit equivalence for the current source. $Z_0 = R_C \parallel 1/h_{0e}$	**Output Impedance** Z_0 is the output impedance when $V_i = 0$. When $V_i = 0, i_b = 0$, resulting in open circuit equivalence for the current source. $Z_0 = R_C \parallel r_o$
Voltage gain A_V $V_0 = -\beta I_b (R_C \parallel r_0)$ From r_e model, $I_b = \frac{V_i}{\beta r_e}$ $V_0 = -\beta \frac{V_i}{\beta r_e}(R_C \parallel r_0)$ $A_V = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_0)}{r_e}$ If $r_0 \geq 10R_C$	**Voltage gain A_V** $V_0 = -h_{fe} I_b (R_C \parallel 1/h_{0e})$ From hybrid model, $I_b = \frac{V_i}{h_{ie}}$ $V_0 = -h_{fe} \frac{V_i}{h_{ie}} (R_C \parallel 1/h_{0e})$ $A_V = \frac{V_o}{V_i} = -h_{fe} \frac{(R_C \parallel 1/h_{0e})}{h_{ie}}$	**Voltage gain A_V** $V_0 = -g_m V_\pi (R_C \parallel r_0)$ From hybrid-π model, $V_i = V_\pi = V_{be}$ $V_0 = -g_m V_i (R_C \parallel r_0)$ $A_V = \frac{V_o}{V_i} = -g_m (R_C \parallel r_o)$

$A_V = -\frac{R_C}{r_e}$		

Emitter-Follower

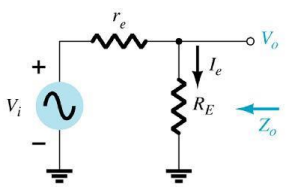


r_e Model



$r_e$model	Hybrid model	Hybrid-π model
Input Impedance Applying KVL to the input side: $$V_i = I_b\beta r_e + I_eR_E$$ $$V_i = I_b\beta r_e + (\beta + 1)I_bR_E$$ Input impedance looking into the network to the right of R_B is $$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$ + = $$Z_b = \frac{V_i}{I_b} = \beta(r_e + R_E)$$ Since $\beta \gg 1$ $(\beta \quad 1) \quad \beta$ Since R_E is often much greater than r_e $$Z_b = \beta r_e$$ $$Z_i = R_B \parallel Z_b$$	**Input Impedance** Applying KVL to the input side: $$V_i = I_bh_{ie} + I_eR_E$$ $$V_i = I_bh_{ie} + (h_{fe} + 1)I_bR_E$$ Input impedance looking into the network to the right of R_B is $$Z_b = \frac{V_i}{I_b} = h_{ie} + h_{fe}R_E$$ Since $h_{fe} \gg h_{ie}$ $$Z_b \cong h_{fe}R_E$$	**Input Impedance** Applying KVL to the input side: $$V_i = I_br_\pi + I_eR_E$$ $$V_i = I_br_\pi + (\beta + 1)I_bR_E$$ Input impedance looking into the network to the right of R_B is $$Z_b = \frac{V_i}{I_b} = r_\pi + (1 + \beta)R_E$$

	$Z_i = R_B \parallel Z_b$	

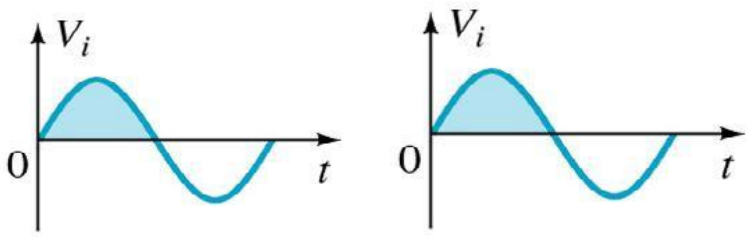
		$Z_i = R_B \parallel Z_b$
Output Impedance To find Zo, it is required to find output equivalent circuit of the emitter follower at its input terminal. This can be done by writing the equation for the current I_b. $I_b = \frac{V_i}{Z_b}$ $I_e = (\beta + 1) I_b$ $= (\beta + 1) \frac{V_i}{Z_b}$ We know that $Z_b = \beta r_e + (\beta + 1) R_E$ Substituting this in the equation of I_e $I_e = (\beta + 1) \frac{V_i}{Z_b}$ $= (\beta + 1)(V_i / \beta r_e + (\beta + 1) R_E)$ Dividing by (β+1) we get $I_e = V_i / \beta r_e + (\beta + 1) + R_E$ Since $(\beta + 1) = \beta$ $I_e = \frac{V_i}{[r_e + R_E]}$ Using the equation $I_e =$ $V_i / [r_e + R_E]$ we can write the output equivalent circuit as,  	**Output Impedance** To find Zo, it is required to find output equivalent circuit of the emitter follower at its input terminal. This can be done by writing the equation for the current I_b. $I_b = \frac{V_i}{Z_b}$ $I_e = (h_{fe} + 1) I_b$ $= (h_{fe} + 1) \frac{V_i}{Z_b}$ We know that $Z_b = h_{ie} + (h_{fe} + 1) R_E$ Substituting this in the equation of I_e $I_e = (h_{fe} + 1) \frac{V_i}{Z_b}$ $= (h_{fe} + 1) \frac{V_i}{h_{ie} + (h_{fe} + 1) R_E}$ Constructing the network as defined by the eq. As per the equivalent circuit	**Output Impedance** To find Zo, it is required to find output equivalent circuit of the emitter follower at its input terminal. This can be done by writing the equation for the current I_b. $I_b = \frac{V_i}{Z_b}$ $I_e = (\beta + 1) I_b$ $= (\beta + 1) \frac{V_i}{Z_b}$ We know that $Z_b = r_\pi + (1 + \beta) R_E$ Substituting this in the equation of I_e $I_e = (\beta + 1) \frac{V_i}{Z_b}$ $I_e = (\beta + 1) \frac{V_i}{r_\pi + (1 + \beta) R_E}$ Constructing the network as defined by the eq. As per the equivalent circuit

As per the equivalent circuit $$Z_0 = r_e \parallel R_E$$		

Since R_E is typically much greater than r_e $\boldsymbol{Z_0 \cong r_e}$	$Z_o = R_E \parallel \frac{h_{ie}}{1+h_{fe}}$ $Z_o \cong R_E \parallel \frac{h_{ie}}{h_{fe}}$	$Z_o = R_E \parallel \frac{r_\pi}{1+\beta}$ $Z_o \cong R_E \parallel \frac{r_\pi}{\beta}$
Voltage gain Using voltage divider rule for the equivalent circuit $V_o = iR_E/(R_E + r_e)\ V$ $A_V = V_o/V_i = [R_E/(R_E + r_e)$ Since$(R_E + r_e) \cong R_E$ $A_V = V_o/V_i \cong R_E/R_E \cong 1$	**Voltage gain** Using voltage divider rule for the equivalent circuit $V_0 = \frac{V_i R_E}{R_E + (h_{ie}/1+h_{fe})}$ $A_V = V_o/V_i$ $= \frac{R_E}{R_E + (h_{ie}/1+h_{fe})}$ As $h_{ie} \ll h_{fe}$ $A_V = V_o/V_i \cong 1$	**Voltage gain** Using voltage divider rule for the equivalent circuit $V_0 = \frac{V_i R_E}{R_E + r_\pi/1+\beta}$ $A_V = V_o/V_i$ $= \frac{R_E}{R_E + r_\pi/1+\beta}$ As $r_\pi \ll \beta$ $A_V = V_o/V_i \cong 1$

Phase Shift

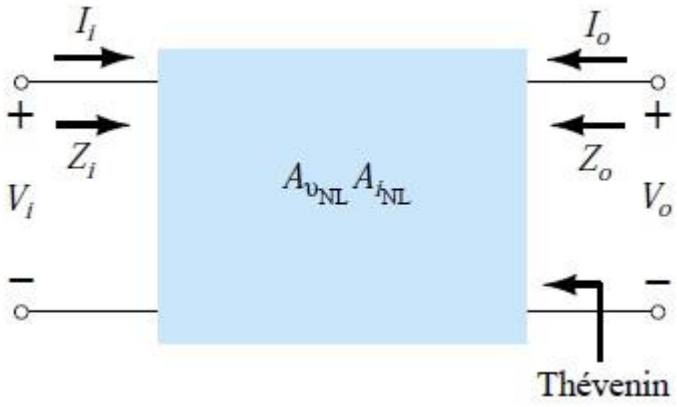
As seen in the gain equation, output and input are in phase.



Effects of R_s and R_L

Two-Port Network

- ✓ The description of BJTs and FETs can be applied to any two-port system.
- ✓ Fig. shows, the important parameters of a two-port system.



- ✓ The impedance levels and the gains of Fig. are determined for no-load (absence ofR_L) and no-source resistance (R_S) conditions.

- ✓ If we take a "Thevenin look" at the output terminals we find with V_i set to zero that

$$Z_{Th} = Z_0 = R_0$$

- ✓ E_{Th} is the open-circuit voltage between the output terminals identified asV_0 . However

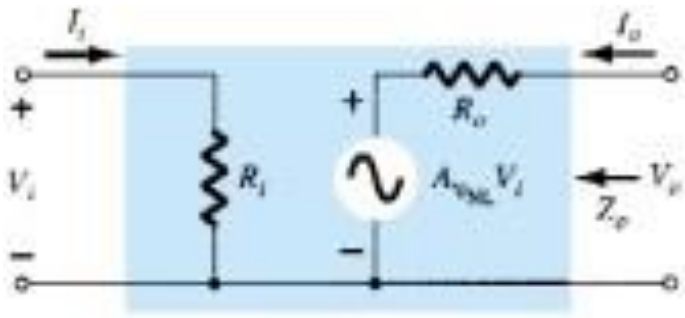
$$A_{VNL} = \frac{V_0}{V_i}$$

$$V_0 = A_{VNL} V_i$$

So that $$E_{Th} = A_{VNL} V_i$$

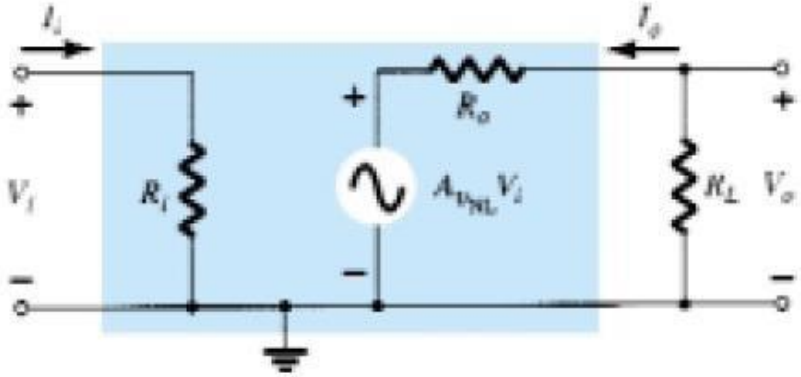
Note the use of the additional subscript notation "NL" to identify a no-load voltage gain.

- ✓ Substituting the Thevenin equivalent circuit between the output terminals will result in the output configuration of Fig.



Effect of a Load Impedance (R_L)

- ✓ The effect of an applied load using the two-port model is shown in Fig.
- ✓ The model can be applied to any current- or voltage-controlled amplifier.



- ✓ A_{VNL} is, as defined earlier, the gain of the system without an applied load. $R_I$and $R_0$are the input and output impedances of the amplifier as defined by the configuration.
- ✓ Ideally, all the parameters of the model are unaffected by changing loads and source resistances.
- ✓ Applying the voltage-divider rule to the output circuit will result in

$$V_0 = \frac{R_L A_{VNL} V_i}{R_L + R_0}$$

$$A_V = \frac{V_0}{V_i} = \frac{R_L}{R_L + R_0} A_{VNL}$$

Current gain(A_i)

- ✓ The applied voltage and input current will always be related by

$$I_i = \frac{V_i}{Z_i} = \frac{V_i}{R_i}$$

- ✓ The output current as the current through the load will result in

$$I_0 = -\frac{V_0}{R_L}$$

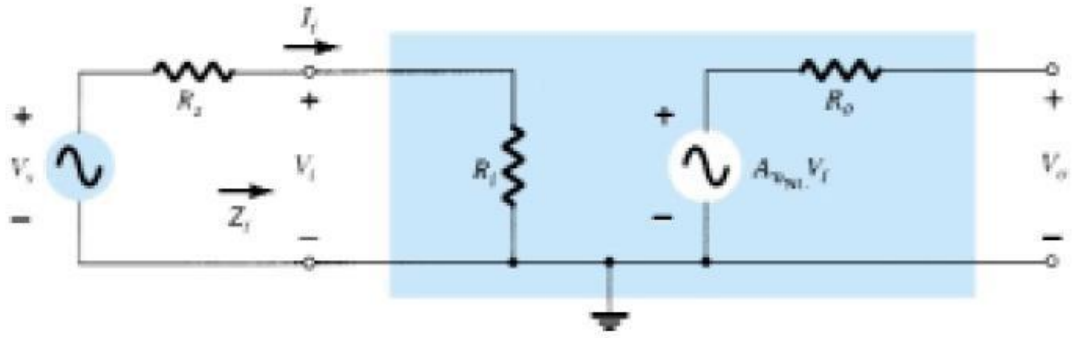
- ✓ The current gain is then determined by

$$A_i = \frac{I_0}{I_i} = -\frac{V_0/R_L}{V_i/Z_i} = -\frac{V_0}{V_i}\frac{Z_i}{R_L}$$

$$\boxed{A_i = -A_V \frac{Z_i}{R_L}}$$

Effect of the Source Impedance (R_S)

- ✓ In Fig., a source with an internal resistance has been applied to the basic twoport system.



- ✓ The fraction of the applied signal reaching the input terminals of the amplifier of Fig. is determined by the voltage-divider rule.

$$V_i = \frac{R_i V_S}{R_i + R_S}$$

- ✓ For the two-port system of Fig.

$$V_0 = A_{VNL} V_i$$

$$V_i = \frac{R_i V_S}{R_i + R_S}$$

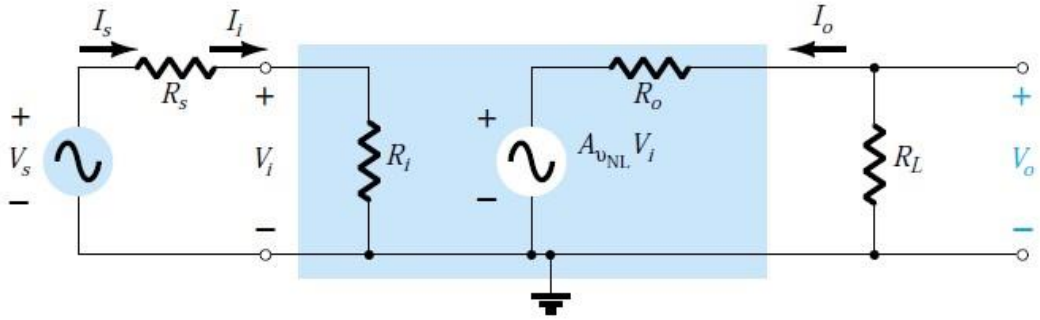
$$V_0 = A_{VNL} \frac{R_i V_S}{R_i + R_S}$$

Voltage gain with source resistance R_S

$$A_{V_S} = \frac{V_0}{V_S} = \frac{R_i}{R_i + R_S} A_{VNL}$$

COMBINED EFFECT OF R_S AND R_L

- ✓ In Fig, a source with an internal resistance R_S and a load R_L have been applied to a two-port system for which the parameters Z_i, A_{VNL}, and Z_0 have been specified.



- ✓ At the input side we find

$$V_i = \frac{R_i V_S}{R_i + R_S}$$

$$\frac{V_i}{V_S} = \frac{R_i}{R_i + R_S}$$

- ✓ At the output side

$$V_0 = \frac{R_L A_{VNL} V_i}{R_L + R_0}$$

$$A_V = \frac{V_0}{V_i} = \frac{R_L A_{VNL}}{R_L + R_0}$$

- ✓ For the total gain $A_{V_S} = \frac{V_0}{V_S}$, the following mathematical steps can be performed:

$$A_{V_S} = \frac{V_0}{V_S} = \frac{V_0}{V_i}\frac{V_i}{V_S}$$

$$A_{V_S} = \frac{R_L A_{VNL}}{R_L + R_0}\frac{R_i}{R_i + R_S}$$

$$A_{V_S} = \frac{V_0}{V_S} = \frac{R_i}{R_i + R_S}\frac{R_L}{R_L + R_0} A_{VNL}$$

Small Signal Analysis of FETs

Prepared by:

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Assistant Professor

Department of Electrical Engineering

GCE, Keonjhar

Reference: **"Electronic Devices and Circuit Theory"**

Robert L. Boylestad and L. Nashelsky

FET Small-Signal Analysis

Transconductance

- ✓ The control that V_{GS}over the drain current I_D is measured by transconductance.
- ✓ It is denoted asg_m.
- ✓ It may be defined as the ratio of change in drain current to the change in gatesource voltage V_{GS} at constantV_{DS}.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} = constant$$

Mathematical definition of g_m

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{dI_D}{dV_{GS}}$$

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_p})^2$$

$$\frac{dI_D}{dV_{GS}} = I_{DSS}2\left(1 - \frac{V_{GS}}{V_P}\right)(-\frac{1}{V_P})$$

$$g_m = \frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Substituting $V_{GS} = 0$ in the above equation we get

$$g_{mo} = -\frac{2I_{DSS}}{V_P}, V_{GS} = 0$$

$$\boldsymbol{g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)}$$

JFET Impedance

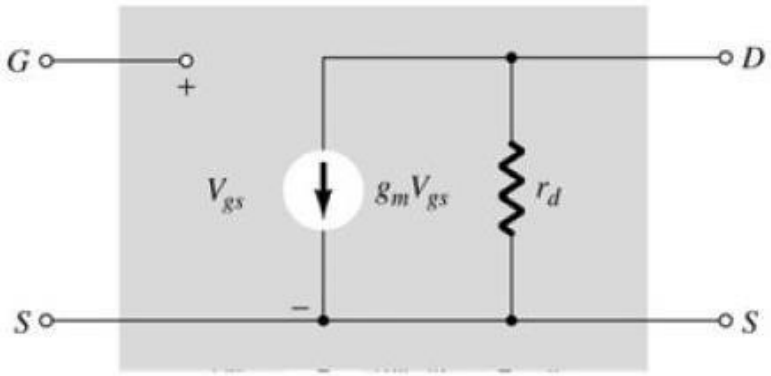
Input Impedance $Z_i = \infty\ ohms$

Output Impedance Z_o: $r_d = 1/y_{os}$

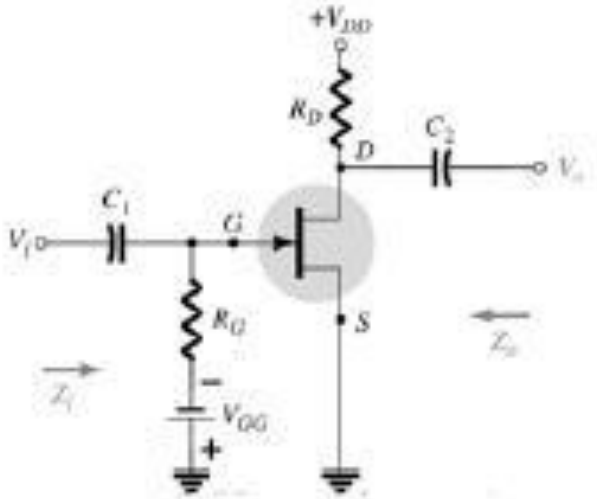
$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} = constant$$

y_{os}: Admittance equivalent circuit parameter listed on FET specification sheets.

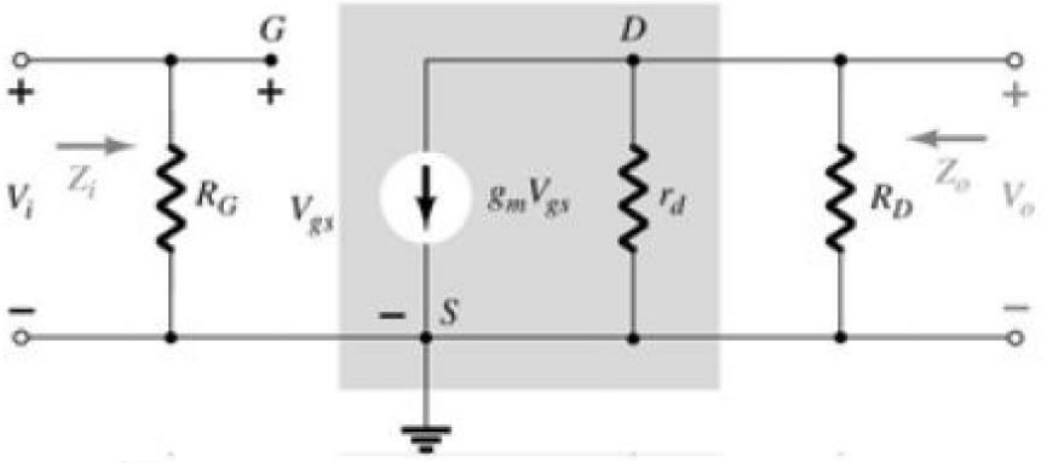
FET AC Equivalent Circuit



JFET Common-Source (CS) Fixed-Bias Configuration



- ✓ The input is on the gate and the output is on the drain.
- ✓ Fixed bias configuration includes the coupling capacitors C_1 and C_2 that isolates the dc biasing arrangements from the applied signal and load.
- ✓ They act as short circuit equivalents for the ac analysis. **AC Equivalent Circuit**



Input Impedance

$$Z_i = R_G$$

Output Impedance

Setting $V_i = 0V$ as required by the defination of Z_o will establish V_{gs}as 0V also. The result is$g_m V_{gs} = 0mA$, current source can be replaced by an open circuit equivalent. The output impedance is

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D, r_d \geq 10R_D$$

Voltage gain

Solving for V_0we get

$$V_o = -g_m V_{gs}(R_D \parallel r_d)$$

But$V_{gs} = V_i$

$$V_o = -g_m V_i(R_D \parallel r_d)$$

$$A_V = \frac{V_o}{V_i} = -g_m (R_D \parallel r_d)$$

If $r_d \geq 10R_D$

$$A_V = -g_m R_D$$

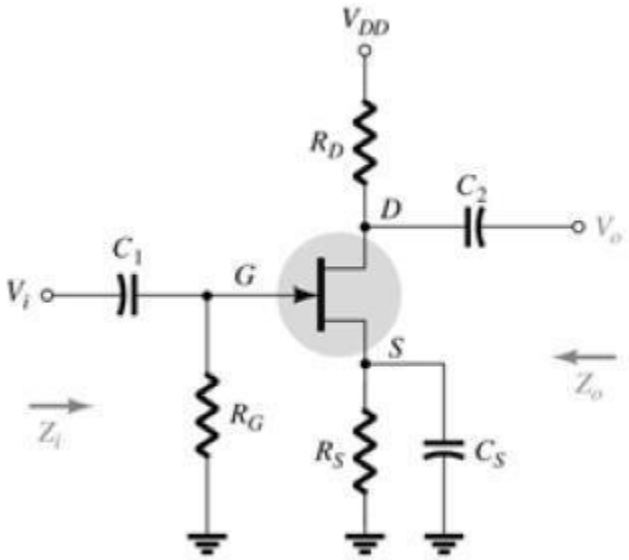
Phase difference

Negative sign in the gain expression indicates that the output voltage is 180^0 phase shifted to that of input.

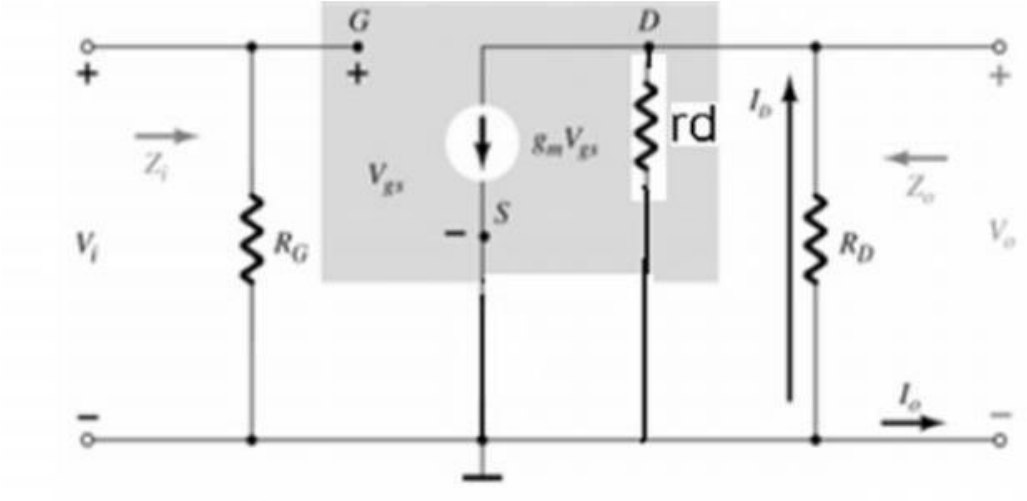
JFET Self bias configuration

- ✓ Main disadvantage of fixed bias configuration requires two dc voltage sources.
- ✓ Self bias circuit requires only one DC supply to establish the desired operating point.

Bypassed R_S



AC equivalent circuit



Input Impedance

$$Z_i = R_G$$

Output Impedance

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D, r_d \geq 10R_D$$

Voltage gain

$$A_V = \frac{V_o}{V_i} = -g_m(R_D \parallel r_d)$$

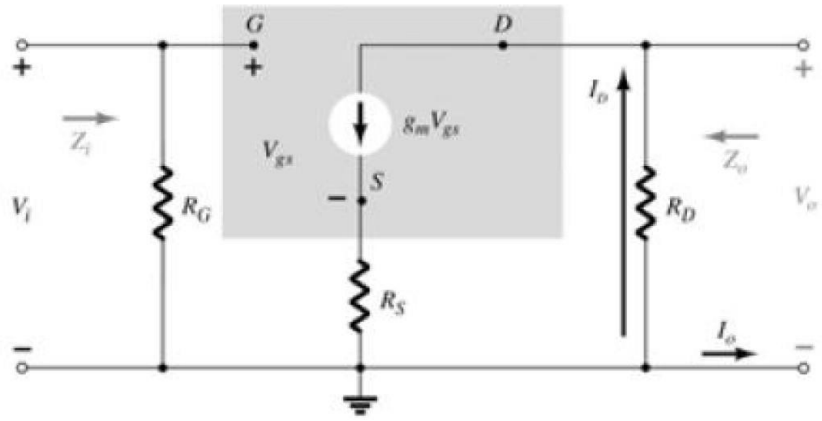
If $r_d \geq 10R_D$

$$A_V = -g_m R_D$$

Phase difference

Negative sign in the gain expression indicates that the output voltage is 180^0 phase shifted to that of input.

Unbypassed R_S



- ✓ Here R_S is part of the equivalent circuit.
- ✓ There is no way to reduce the network with lowest complexity.
- ✓ Carefully all the parameters have to be calculated by considering all polarities properly.

Input Impedance

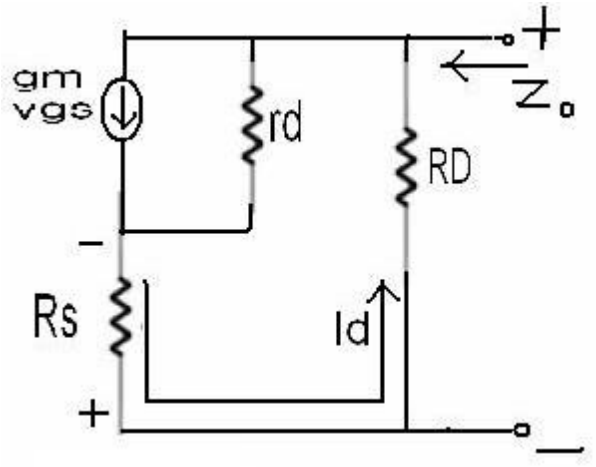
Due to open-circuit condition between gate and output network, the input impedance remains as follows:

$$Z_i = R_G$$

Output Impedance

$$Z_0 = R_D$$

Including the effects of r_d



Output Impedance

$$Z_0 = \frac{[1 + g_m R_S + \frac{R_S}{r_d}]}{[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}]} R_D$$

If $r_d \geq 10R_D$

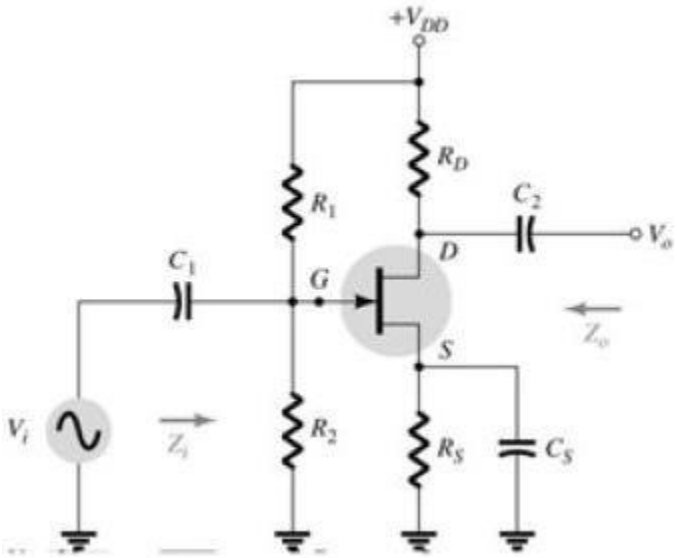
$$Z_0 \cong R_D$$

Voltage gain

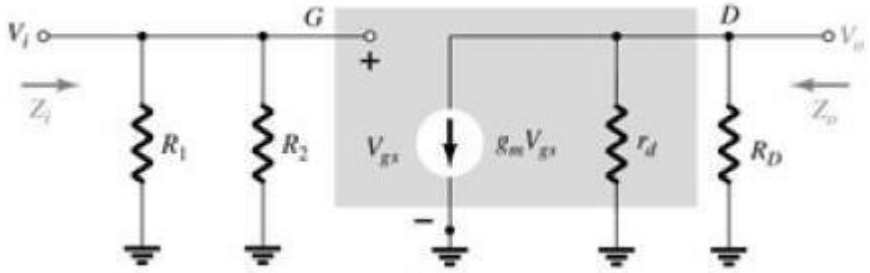
$$A_V = \frac{V_0}{V_i} = \frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

If $r_d \geq 10R_D$ $A_V = \frac{V_0}{V_i} = \frac{g_m R_D}{1+g_m R_S}$

JFET voltage divider configuration



AC equivalent circuit



Input Impedance

$$Z_i = R_1 \parallel R_2$$

Output Impedance

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D, r_d \geq 10R_D$$

Voltage gain

$$V_o = -g_m V_{gs}(R_D \parallel r_d)$$

But $V_{gs} = V_i$

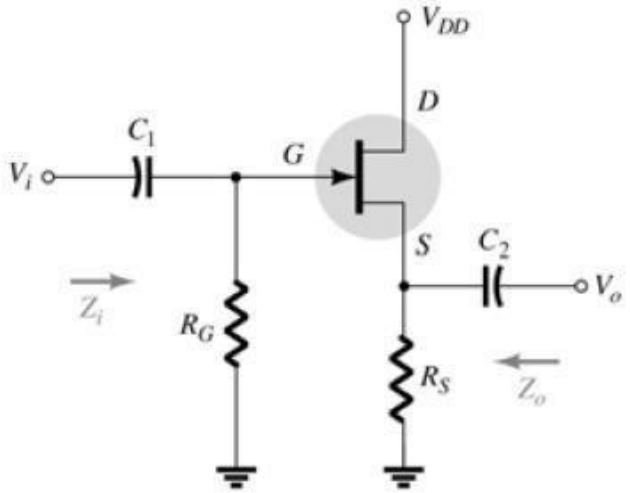
$$V_o = -g_m V_i(R_D \parallel r_d)$$

$$A_V = \frac{V_o}{V_i} = -g_m (R_D \parallel r_d)$$

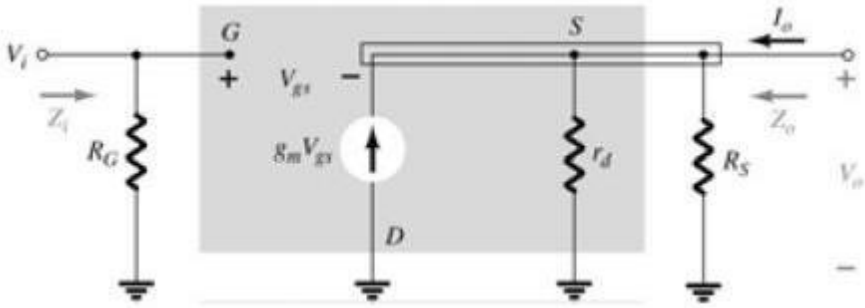
If $r_d \geq 10R_D$

$$A_V = -g_m R_D$$

JFET source follower



AC equivalent circuit



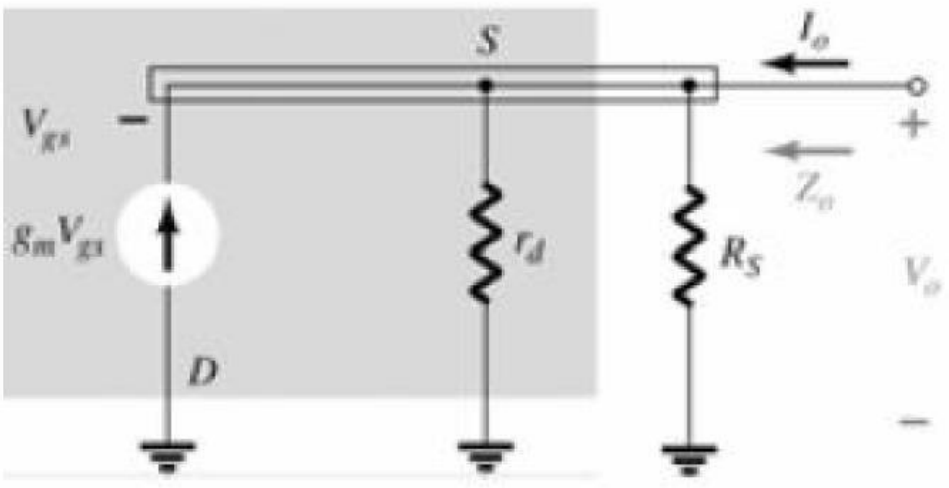
Input Impedance

$$Z_i = R_G$$

Output Impedance

Setting V_i=0V will result in the gate terminal being connected directly to ground as shown in figure below.

Equivalent circuit



Applying KCL at output node

$$I_o + g_m V_{gs} = I_{rd} + I_{rs}$$

$$= \frac{V_0}{r_d} + \frac{V_0}{R_S}$$

The result is $$I_0 = V_0\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$

$$= V_0\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_0]$$

$$= V_0\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

$$Z_0 = \frac{V_0}{I_0} = \frac{V_0}{V_0\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]}$$

$$= \frac{1}{\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]}$$

$$= \frac{1}{\left[\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}\right]}$$

$$Z_0 = r_d \parallel R_S \parallel g_m$$

For $r_d \geq 10R_S$

$$Z_0 \cong r_d \parallel 1/g_m$$

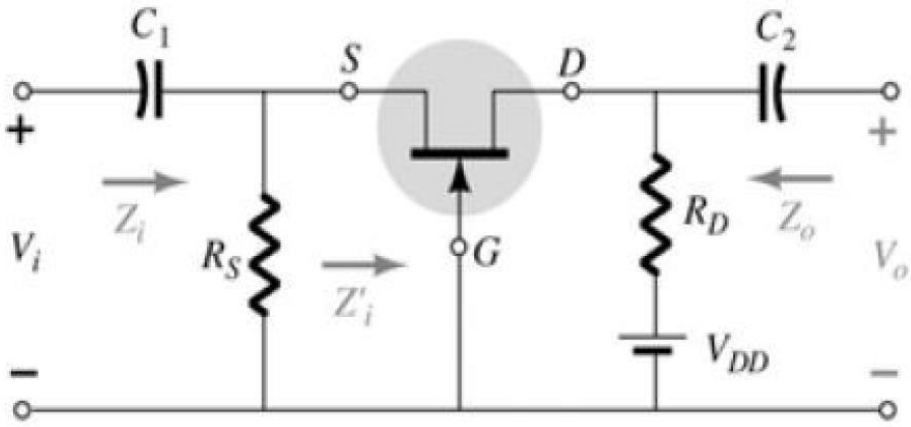
Voltage gain

$$A_V = \frac{V_0}{V_i} = \frac{g_m(r_d \parallel R_S)}{1 + g_m(r_d \parallel R_S)}$$

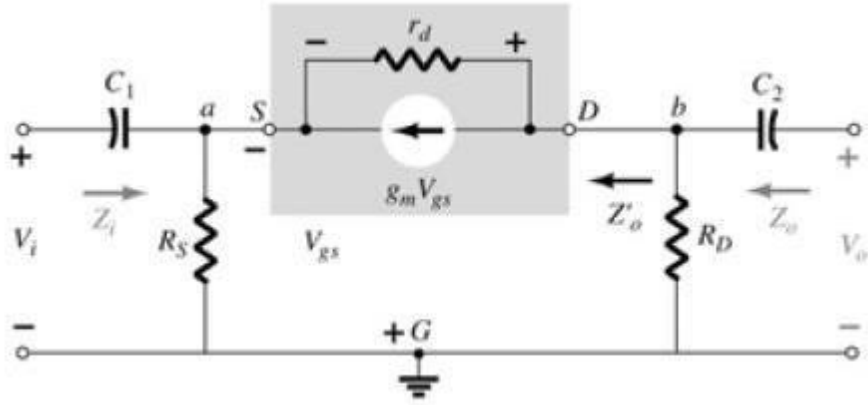
For $r_d \geq 10R_S$

$$A_V = \frac{V_0}{V_i} = \frac{g_m R_S}{1 + g_m R_S}$$

JFET common gate configuration



AC equivalent circuit



Input Impedance

$$Z_i = R_S \parallel \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$$

For $r_d \geq 10R_D$,

$$Z_i \cong R_S \parallel 1/g_m$$

Output Impedance

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D, r_d \geq 10R_D$$

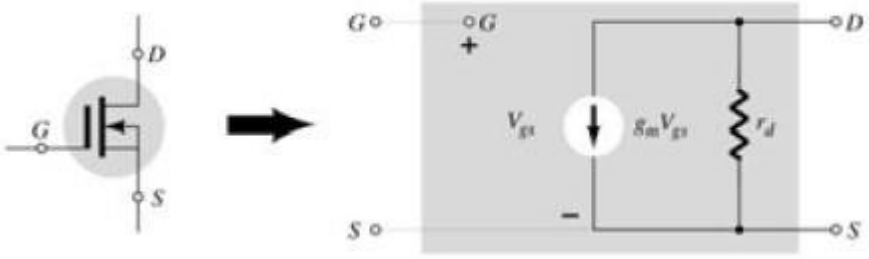
Voltage gain

$$A_V = \frac{V_0}{V_i} = \frac{[g_m R_D + \frac{R_D}{r_d}]}{1 + \frac{R_D}{r_d}}$$

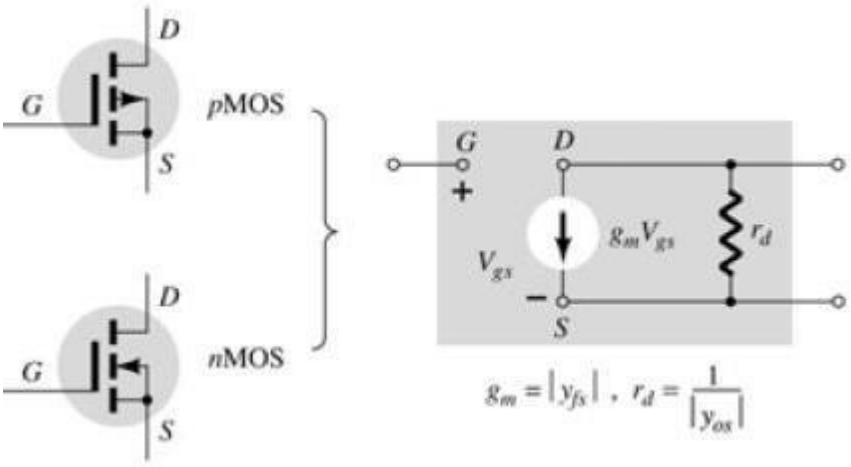
For $r_d \geq 10R_D$

$$A_V \cong g_m R_D$$

D-MOSFET ac equivalent model

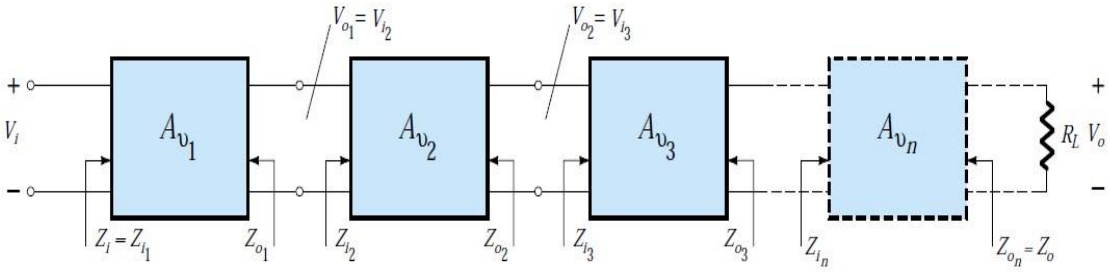


E-MOSFET ac small signal model



CASCADED SYSTEMS

- ✓ The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig., whereA_{V1},A_{V2},A_{V3}, and so on, are the voltage gains of each stage *under loaded conditions*.



- ✓ That is, $A_{V1}$is determined with the input impedance to A_{V2}acting as the load onA_{V1}.

- ✓ ForA_{V2}, A_{V1}will determine the signal strength and source impedance at the input toA_{V2}.

- ✓ The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{VT} = A_{V1}.\ A_{V2}.\ A_{V3} \ldots \ldots \ldots$$

- ✓ The total current gain by

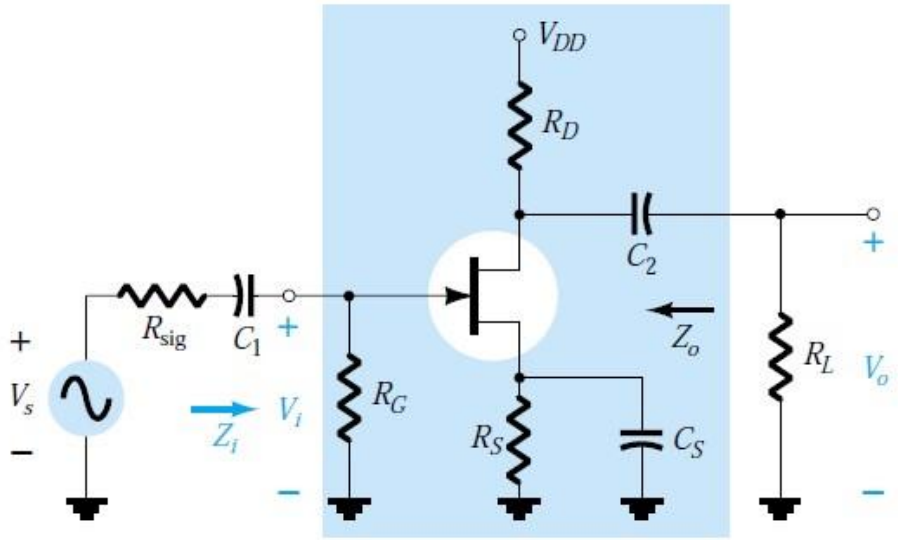
$$A_{i_T} = -A_{V_T}\frac{Z_{i_1}}{R_L}$$

Effects of R_{Sig} and R_L on CS amplifier

✓ The isolation that exists between gate and drain or source of an FET amplifier ensures that changes in R_L do not affect the level of $Z_i$and changes in R_{Sig}do not affectR_0.

Bypassed Source Resistance

✓ For the FET amplifier of Fig, the applied load will appear in parallel with $R_D$in the small-signal model.



✓ The equation for the loaded gain is given by :

$$A_V = -g_m(R_D \parallel R_L)$$

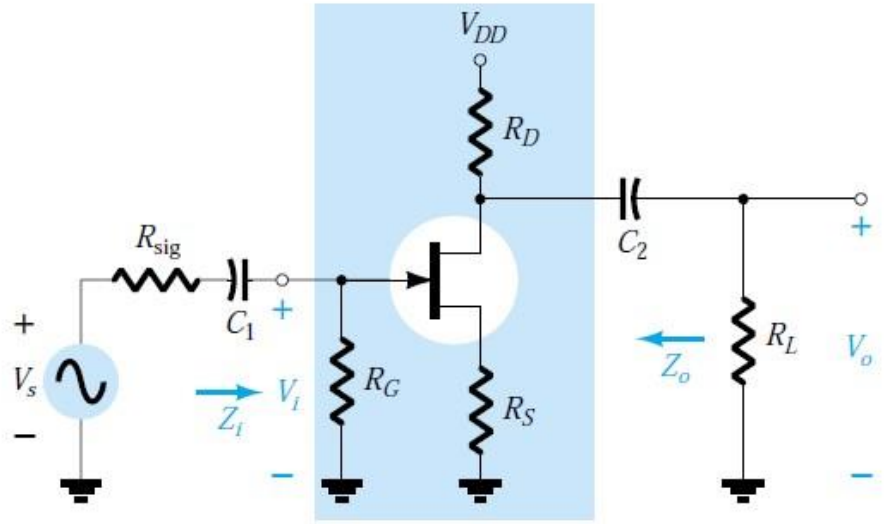
✓ The impedance levels remain at

$$Z_i = R_G$$

$$Z_0 = R_D$$

Unbypassed Source Resistance

✓ For the FET amplifier of Fig., the load will again appear in parallel withR_D.



✓ The equation for the loaded gain is given by :

$$A_V = \frac{V_0}{V_i} = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$$

✓ The impedance levels remain at

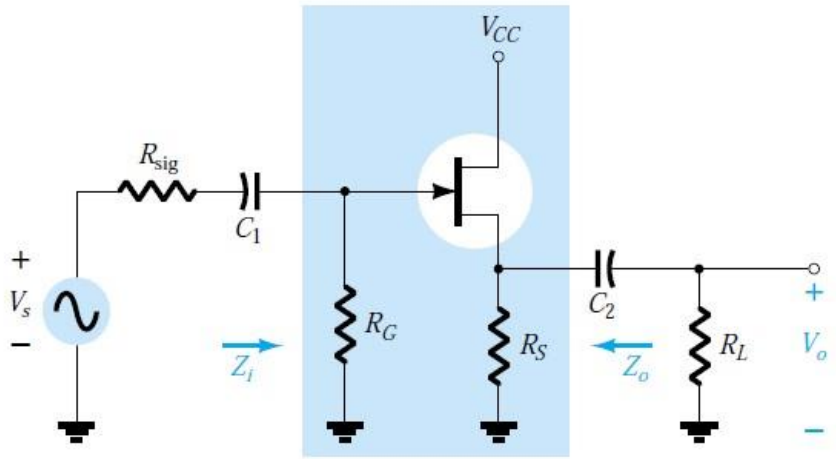
$$Z_i = R_G$$

$$Z_0 = R_D$$

Source Follower

✓ For the source-follower configuration of Fig., the level of $Z_i$is independent of the magnitude of $R_L$and determined by

$$Z_i = R_G$$



- ✓ The loaded voltage gain has the same format as the unloaded gain with $R_S$replaced by the parallel combination of $R_S$andR_L.

$$A_V = \frac{V_0}{V_i} = \frac{g_m(R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)}$$

- ✓ The level of output impedance is

$$Z_0 = R_S \parallel \frac{1}{g_m}$$

High Frequency Response of FETs and BJTs

Prepared by:

DEBASISH MOHANTA
Assistant Professor
Department of Electrical Engineering
GCE, Keonjhar

Reference: **"Electronic Devices and Circuit Theory"**
Robert L. Boylestad and L. Nashelsky

TRANSISTOR FREQUENCY RESPONSE

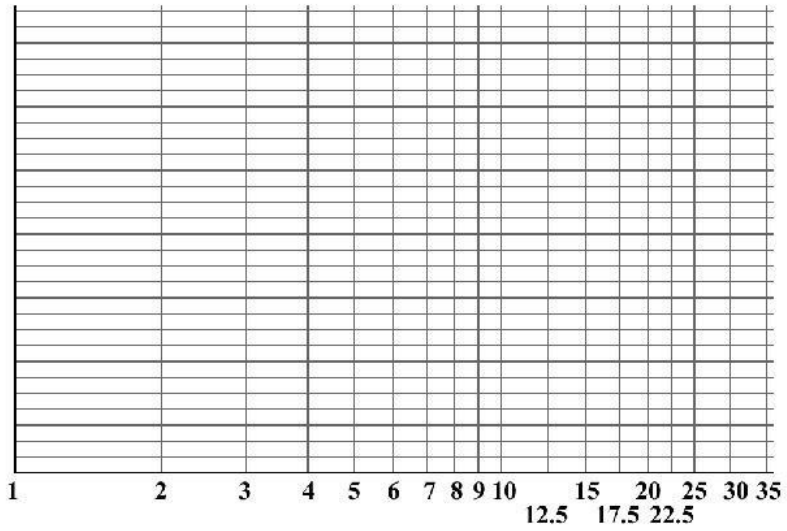
Introduction

It is required to investigate the frequency effects introduced by the larger capacitive elements of the network at low frequencies and the smaller capacitive elements of the active device at high frequencies. Since the analysis will extend through a wide frequency range, the logarithmic scale will be used.

Natural Logarithm (or base e)

- ✓ There is another logarithm that is also useful (and in fact more common in natural processes). Many natural phenomenon are seen to exhibit changes that are either exponentially decaying (radioactive decay for instance) or exponentially increasing (population growth for example).
- ✓ These exponentially changing functions are written as *ea*, where 'a' represents the rate of the exponential change.
- ✓ In such cases where exponential changes are involved, we usually use another kind of logarithm called natural logarithm. The natural log can be thought of as Logarithm Base-e.
- ✓ This logarithm is labeled with ln (for "natural log"), where, e = 2.178.

Semi-Log graph



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Decibels

- ✓ The term decibel has its origin in the fact that the power and audio levels are related on a logarithmic basis. The term bel is derived from the surname of Alexander Graham Bell.

- ✓ bel is defined by the following equation relating two power levels, P1 and P2:

$$G = [\log_{10} P2 / P1] \text{ bel}$$

- ✓ It was found that, the Bel was too large a unit of measurement for the practical Purposes, so the decibel (dB) is defined such that 10 decibels = 1 bel.

- ✓ Therefore,

$$\mathbf{G_{dB} = [10 \log_{10} P2 / P1]\ dB}$$

- ✓ The decimal rating is a measure of the difference in magnitude between two power levels.

- ✓ For a specified output power P2, there must be a reference power level P1. The reference level is generally accepted to be 1mW.

$$\mathbf{G_{dBm} = [10 \log_{10} P2 / 1mW]\ dBm}$$

$$G_{dB} = [10 \log_{10} P2 / P1]\ dB$$

$$= [10 \log_{10} (V_{22} / R_i) / (V_{12} / R_i)]\ dB$$

$$= 10 \log_{10} (V_2 / V_1)2$$

$$\mathbf{G_{dB} = [20 \log_{10} V_2 / V_1]\ dB}$$

One of the advantages of the logarithmic relationship is the manner in which it can be applied to cascaded stages wherein the overall voltage gain of a cascaded system is the sum of individual gains in dB.

$$\mathbf{A_V = (Av1)(Av2)(Av3)…….}$$

$$\mathbf{A_V\ dB = (Av1dB)+(Av2dB)+(Av3dB)…….}$$

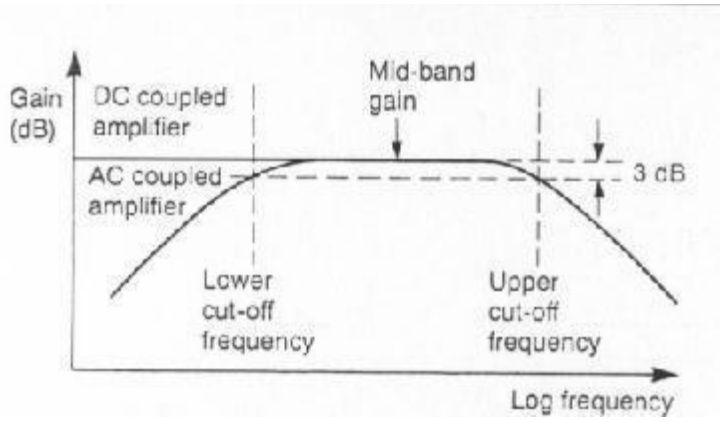
General Frequency considerations

- ✓ At low frequencies the coupling and bypass capacitors can no longer be replaced by the short-circuit approximation because of the increase in reactance of these elements.

- ✓ The frequency-dependent parameters of the small signal equivalent circuits and the stray capacitive elements associated with the active device and the network will limit the high frequency response of the system.

- ✓ An increase in the number of stages of a cascaded system will also limit both the high and low frequency response.

- ✓ The horizontal scale of frequency response curve is a logarithmic scale to permit a plot extending from the low to the high frequency.



- ✓ For the RC coupled amplifier, the drop at low frequencies is due to the increasing reactance of C_C and C_E, whereas its upper frequency limit is determined by either the parasitic capacitive elements of the network or the frequency dependence of the gain of the active device.

- ✓ In the frequency response, there is a band of frequencies in which the magnitude of the gain is either equal or relatively close to the mid band value.

- ✓ To fix the frequency boundaries of relatively high gain, $0.707A_{Vmid}$ is chosen to be the gain at the cutoff levels.

- ✓ The corresponding frequencies f_1 and f_2 are generally called corner, cut off, band, break, or half – power frequencies.

- ✓ The multiplier 0.707 is chosen because at this level the output power is half the mid band power output, that is, at mid frequencies,

$$P_{0mid=}\frac{|V_o{}^2|}{R_0}=\frac{|A_{Vmid}V_i|^2}{R_o}$$

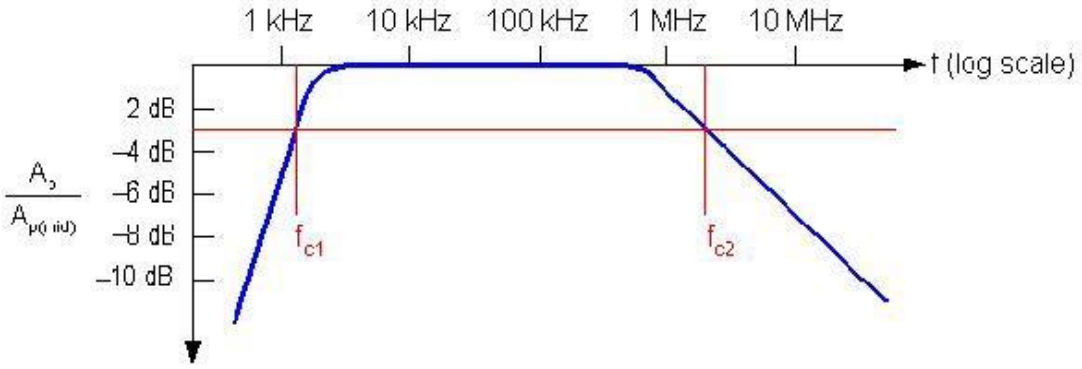
- ✓ And at the half – power frequencies,

$$P_{oHPF=}\frac{|0.707A_{Vmid}V_i|^2}{R_o} = 0.5\frac{|A_{Vmid}V_i|^2}{R_o}$$

$$P_{oHPF} = 0.5P_{0mid}$$

- ✓ The bandwidth of each system is determined by $f_2 - f_1$
- ✓ A decibel plot can be obtained by applying the equation,

$$(Av/Avmid)\ dB = 20\log_{10}(Av/Avmid)$$

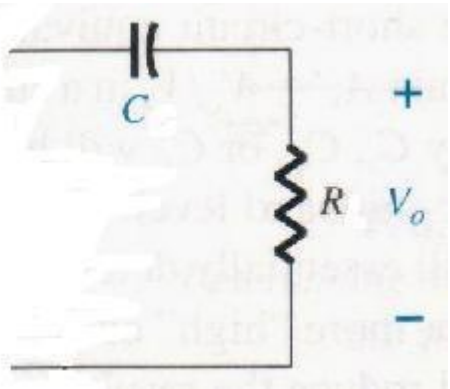


- ✓ Most amplifiers introduce a 180^0 phase shift between input and output signals. At low frequencies, there is a phase shift such that V_0 lags V_i an increased angle. At high frequencies, the phase shift drops below 180^0.

Low-frequency analysis – Bode plot

In the low frequency region of the single-stage BJT amplifier, it is the RC combinations formed by the network capacitors C_C and C_E, the network resistive parameters that determine the cut off frequencies.

Frequency analysis of an RC network



- ✓ Analysis of the above circuit indicates that,

$$X_C = \frac{1}{2\pi fC} \cong 0\Omega$$

- ✓ **Thus, $V_o = V_i$ at high frequencies.**

- ✓ **At f = 0 Hz, $X_C = \infty$, $V_o = 0V$.**

- ✓ Between the two extremes, the ratio, AV = V_0 / V_i will vary. As frequency increases, the capacitive reactance decreases and more of the input voltage appears across the output terminals.

- ✓ The output and input voltages are related by the voltage-divider rule:

$$V_0 = \frac{RV_i}{R+X_C}$$

The magnitude of

$$V_0 = \frac{RV_i}{\sqrt{R^2 + {X_C}^2}}$$

For the special case where $X_C = R$,

$$V_0 = \frac{RV_i}{\sqrt{R^2 + R^2}} = \frac{1}{\sqrt{2}} V_i$$

$$A_V = \frac{V_0}{V_i} = \frac{1}{\sqrt{2}} = 0.707$$

- ✓ The frequency at which this occurs is determined from,

$$X_C = {}^1/_{2\pi f_1 C} = R$$

Where $f_1 = {}^1/_{2\pi RC}$

- ✓ Gain equation is written as,

$$A_V = \frac{V_0}{V_i}$$

$$= {}^{R}/_{(R - jX_C)}$$

$$= \frac{1}{1 - j({}^{1}/_{wCR})}$$

$$= \frac{1}{1 - j({}^{1}/_{2\pi fCR})}$$

$$A_V = \frac{1}{1 - j({}^{f_1}/_{f})}$$

✓ In the magnitude and phase form,

$$A_V = \frac{V_0}{V_i} = \frac{1}{\sqrt{1 + ({}^{f_1}/_{f})^2}} \tan^{-1}({}^{f_1}/_{f})$$

✓ In the logarithmic form, the gain in dB is

$$A_V = \frac{V_0}{V_i} = \frac{1}{\sqrt{1 + ({}^{f_1}/_{f})^2}}$$

$$= 20 \log_{10}[\frac{1}{\sqrt{1 + ({}^{f_1}/_{f})^2}}]$$

$$= -20 \log_{10} \sqrt{1 + ({}^{f_1}/_{f})^2}$$

$$= -\left(\frac{1}{2}\right)(20) \log_{10}[1 + (\frac{f_1}{f})^2]$$

$$= -10 \log_{10}[1 + (\frac{f_1}{f})^2]$$

✓ For frequencies where $f \ll f_1$ or $({}^{f_1}/{f})^2 \gg 1$ can be approximated as

$$A_V(dB) == -10 \log_{10}[(\frac{f_1}{f})^2]$$

$$\boldsymbol{A_V(dB) == -20 \log_{10} \frac{f_1}{f}} \; at \; f \ll f_1$$

✓ At $f = f_1$:

$$\frac{f_1}{f} = 1 \; and$$

$$-20 \log_{10} 1 = 0 \; dB$$

- ✓ At $f = \frac{1}{2} f_1$:

$$\frac{f_1}{f} = 2 \; and$$

$$-20 \log_{10} 2 \cong -6dB$$

- ✓ At $f = \frac{1}{4} f_1$:

$$\frac{f_1}{f} = 4 \; and$$

$$-20 \log_{10} 4 \cong -12dB$$

- ✓ At $f = \frac{1}{10} f_1$:

$$\frac{f_1}{f} = 10 \; and$$

$$-20 \log_{10} 10 \cong -20 \; dB$$

- ✓ The above points can be plotted which forms the Bode- plot.

- ✓ Note that, these results in a straight line when plotted in a logarithmic scale. Although the above calculation shows at f = f_1, gain is 3dB, we know that f1 is that frequency at which the gain falls by 3dB. Taking this point, the plot differs from the straight line and gradually approaches to 0dB by f = $10f_1$.

Observations from the above calculations:

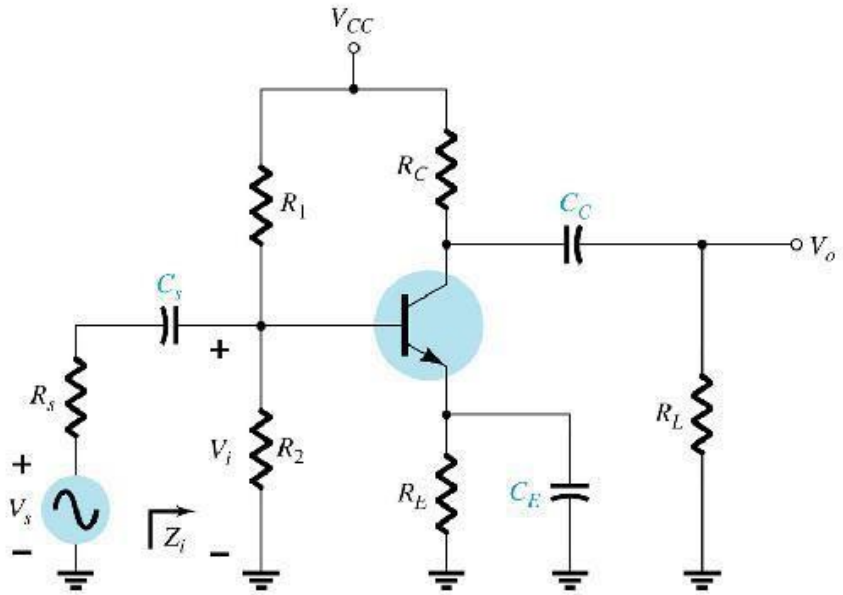
- ✓ When there is an octave change in frequency from $f1 \; / \; 2$ to f_1, there exists corresponding change in gain by 6dB.

- ✓ When there is a decade change in frequency from $f1 \; /10$ to f_1, there exists corresponding change in gain by 20dB.

Low frequency response – BJT amplifier

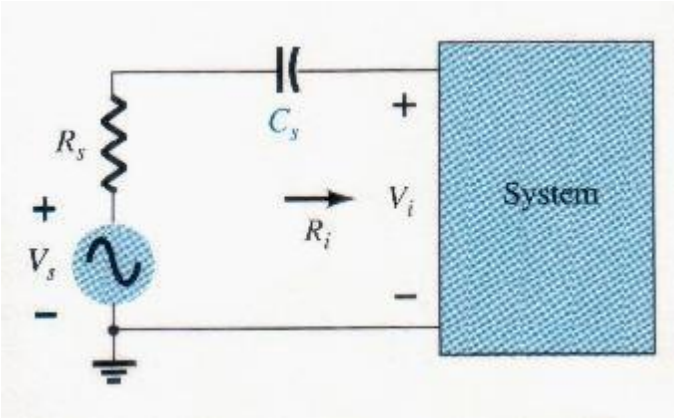
- ✓ A voltage divider BJT bias configuration with load is considered for this analysis.

- ✓ For such a network of voltage divider bias, the capacitors C_S, C_C and C_E will determine the low frequency response.



Let us consider the effect of each capacitor independently.

Effect of C_S:



$$f_{L_S} = \frac{1}{2\pi(R_S + R_i)C_S}$$

$$R_i = R_1 \parallel R_2 \parallel \beta r_e$$

- ✓ At mid or high frequencies, the reactance of the capacitor will be sufficiently small to permit a short-circuit approximations for the element.

- ✓ The voltage Vi will then be related to Vs by

$$V_{i|mid} = V^S R^{i/}(R_S + R_i)$$

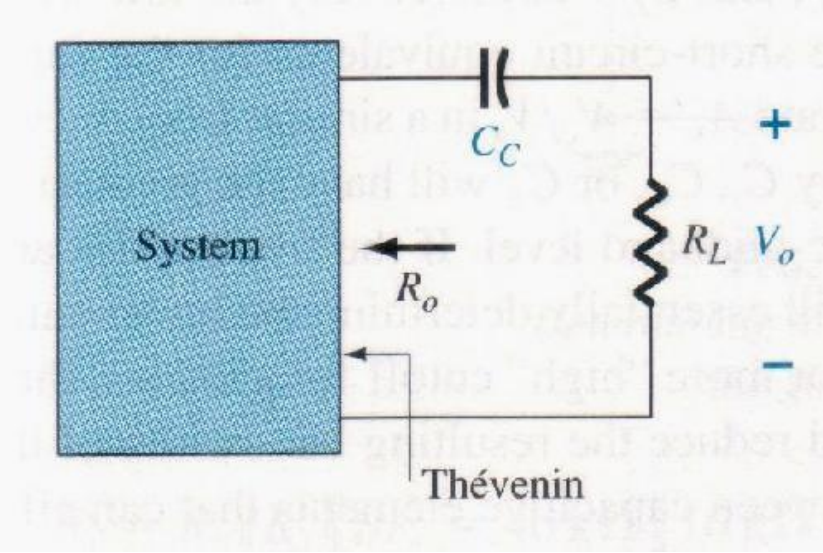
- ✓ At$f = f_{LS}$, V_i =70.7% of its mid band value.

- ✓ The voltage V_i applied to the input of the active device can be calculated using the voltage divider rule:

$$V_i = \frac{R_i V_s}{R_S + R_i - jX_{C_S}}$$

Effect of C_C:

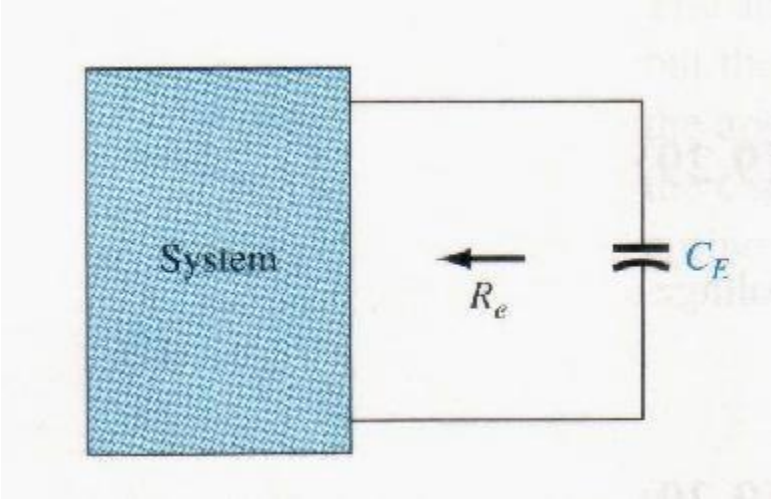
- ✓ Since the coupling capacitor is normally connected between the output of the active device and applied load, the RC configuration that determines the low cut off frequency due to C_C appears as in the figure given below.



$$f_{L_C} = \frac{1}{2\pi(R_0 + R_L)C_C}$$

$$R_0 = R_C \parallel r_0$$

Effect of C_E:



$$f_{L_e} = \frac{1}{2\pi R_e C_E}$$

$$R_e = R_E \parallel (\frac{R_S{}'}{\beta} + r_e)$$

$$R_S{}' = R_S \parallel R_1 \parallel R_2$$

- ✓ The effect of CE on the gain is best described in a quantitative manner by recalling that the gain for the amplifier without bypassing the emitter resistor is given by:

$$A_V = \frac{-R_C}{r_e + R_E}$$

- ✓ Maximum gain is obviously available where R_E is 0Ω.

- ✓ At low frequencies, with the bypass capacitor C_E in its "open circuit" equivalent state, all of R_E appears in the gain equation above, resulting in minimum gain.

- ✓ As the frequency increases, the reactance of the capacitor C_E will decrease, reducing the parallel impedance of R_E and C_E until the resistor R_E is effectively shorted out by C_E.

- ✓ The result is a maximum or mid band gain determined by

$$A_V = \frac{-R_C}{r_e}$$

- ✓ The input and output coupling capacitors, emitter bypass capacitor will affect only the low frequency response.

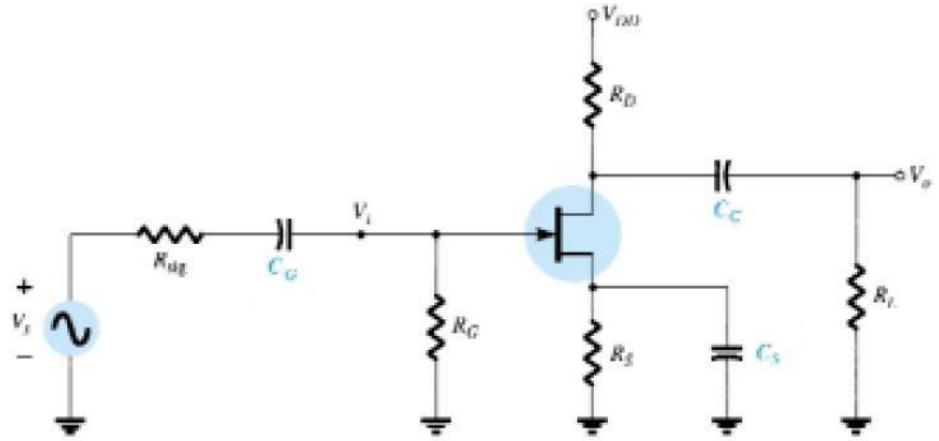
- ✓ At the mid band frequency level, the short circuit equivalents for these capacitors can be inserted.

- ✓ Although each will affect the gain in a similar frequency range, the highest low frequency cut off determined by each of the three capacitors will have the greatest impact.

Low-Frequency Response - FET Amplifier

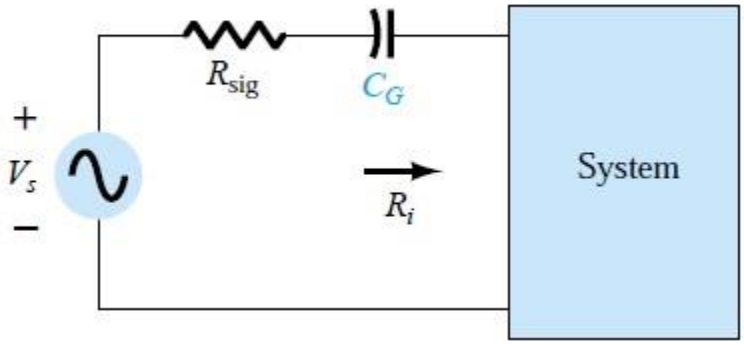
- ✓ The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier.

- ✓ There are again three capacitors of primary concern as appearing in the network of Fig. $C_G, C_C \; and \; C_S$.



Effect of C_G:

- ✓ For the coupling capacitor between the source and the active device, the ac equivalent network will appear as shown in Fig.



- ✓ The cut off frequency determined by C_G will be then

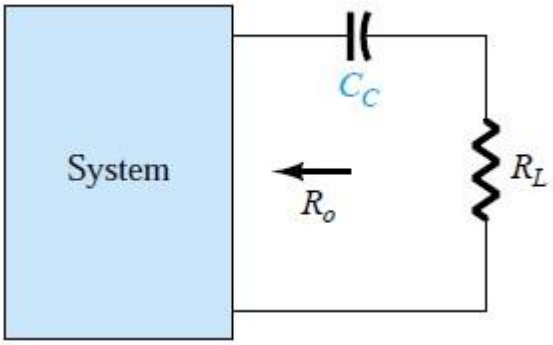
$$f_{L_G} = \frac{1}{2\pi(R_{sig} + R_i)C_G}$$

- ✓ For the network as shown in the above Figure

$$R_i = R_G$$

Effect of C_C:

- ✓ For the coupling capacitor between the active device and the load, the ac equivalent network will appear as shown in Fig.



- ✓ The resulting cut off frequency is

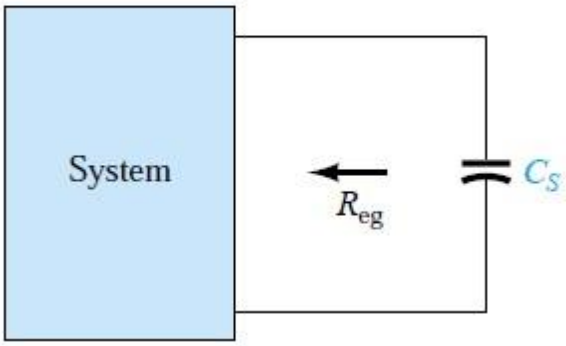
$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}$$

- ✓ For the network as shown in the above Figure

$$R_0 = R_D \parallel r_d$$

Effect of C_S:

- ✓ For the source capacitorC_S, the resistance level of importance is defined by Fig.



- ✓ The cut off frequency will be defined by

$$f_{L_S} = \frac{1}{2\pi R_{eq} C_S}$$

- ✓ From the above network the resulting value of $R_{eq}$is

$$R_{eq} = \frac{R_S}{1 + R_S(1 + g_m r_d)/(r_d + R_D \parallel R_L)}$$

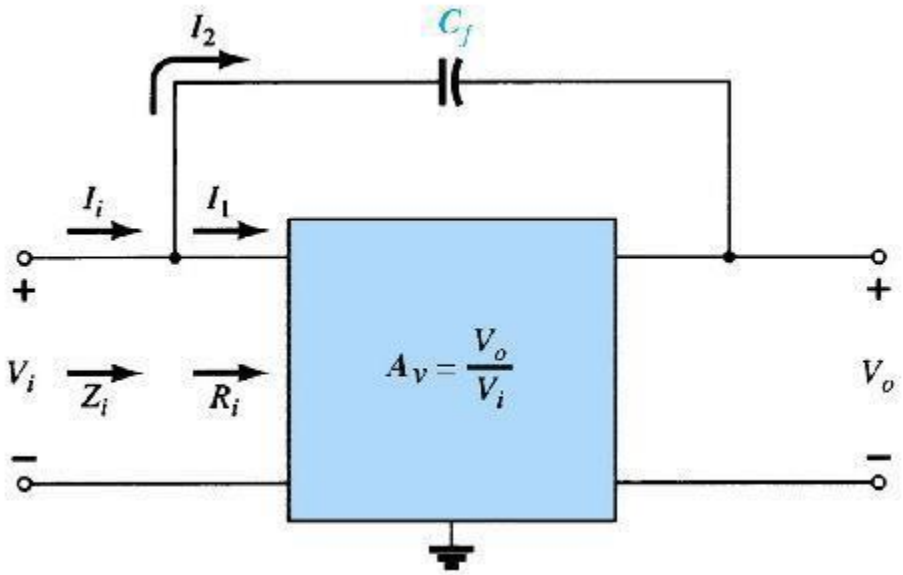
- ✓ For $r_d \cong \infty\Omega$

$$R_{eq} = R_S \parallel \frac{1}{g_m}$$

Miller Effect Capacitance

- ✓ Any P-N junction can develop capacitance.
- ✓ In a BJT amplifier this capacitance becomes noticeable between: the BaseCollector junction at high frequencies in CE BJT amplifier configurations.
- ✓ It is called the Miller Capacitance.

- ✓ It effects the input and output circuits.



- ✓ $I_i = I_1 + I_2$

Using Ohm's law yields

$$I_i = \frac{V_i}{Z_i}$$

$$I_1 = \frac{V_i}{R_i}$$

$$I_2 = (V_i - V_0)/X_{Cf}$$

$$= (V_i - A_V V_i)/X_{Cf}$$

$$I_2 = V_i(1 - A_V)/X_{Cf}$$

Substituting for I_i, I_1 and I_2 in the equation

$$V_i/Z_i = \frac{V_i}{R_i} + V_i(1 - A_V)/X_{Cf}$$

$$1/Z_i = \frac{1}{R_i} + (1 - A_V)/X_{Cf}$$

$$1/Z_i = \frac{1}{R_i} + 1/[\frac{1 - A_V}{X_{Cf}}]$$

$$1/Z_i = \frac{1}{R_i} + \frac{1}{X_{CM}}$$

Where $X_{CM} = [$
$X^{Cf}/(1 - A_V)]$

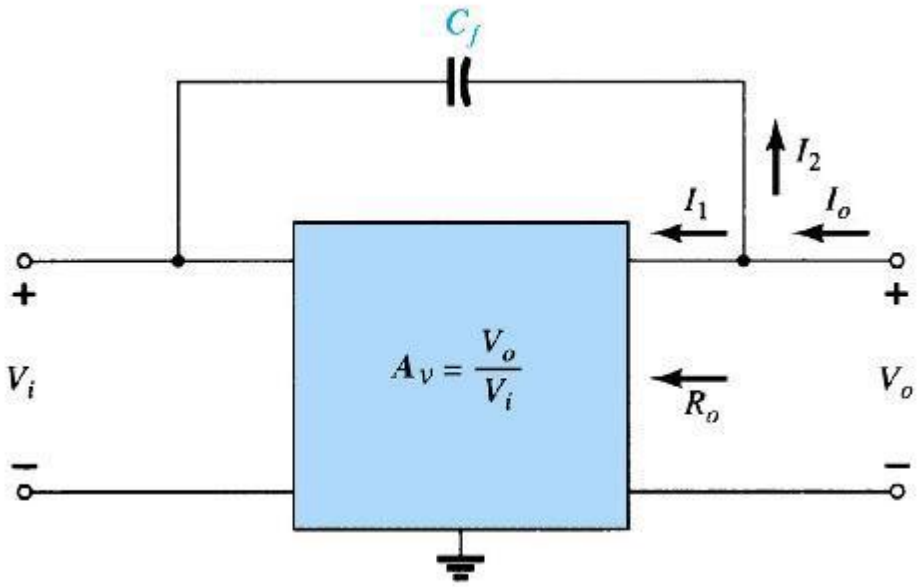
$$= 1/[w(1 - A_V)C_f]$$

$$\boldsymbol{C_{Mi} = (1 - A_V)C_f}$$

C_{Mi} is the Miller effect capacitance.

- ✓ For any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the inter-electrode (parasitic) capacitance between the input and output terminals of the active device.

Miller Output Capacitance



$$C_{M0} \cong C_f$$

Applying KCL at the output node results in:

$$I_0 = I_1 + I_2$$

$$I_1 = \frac{V_0}{R_0}$$

$$I_2 = (V_0 - V_i)/X_{Cf}$$

The resistance Ro is usually sufficiently large to permit ignoring the first term of the equation, thus

$$I_0 \cong (V_0 - V_i)/X_{Cf}$$

Substituting $V_i = V^0/A_V$ from $A_V = V_0/V_i$ results in

$$I_0 = \frac{V_0 - {}^{V_0}/_{A_V}}{X_{C_f}} = \frac{V_0(1 - {}^{1}/_{A_V})}{X_{C_f}}$$

$$\frac{I_0}{V_0} = \frac{(1 - {}^{1}/_{A_V})}{X_{C_f}}$$

$$\frac{V_0}{I_0} = \frac{X_{C_f}}{(1 - {}^{1}/_{A_V})} = \frac{1}{wC_f(1 - {}^{1}/_{A_V})} = \frac{1}{wC_{M_0}}$$

$$\boldsymbol{C_{M_0} = (1 - \frac{1}{A_V})C_f}$$

For the ideal situation where $A_V \gg 1$

$$\boldsymbol{C_{M0} \cong C_f}$$

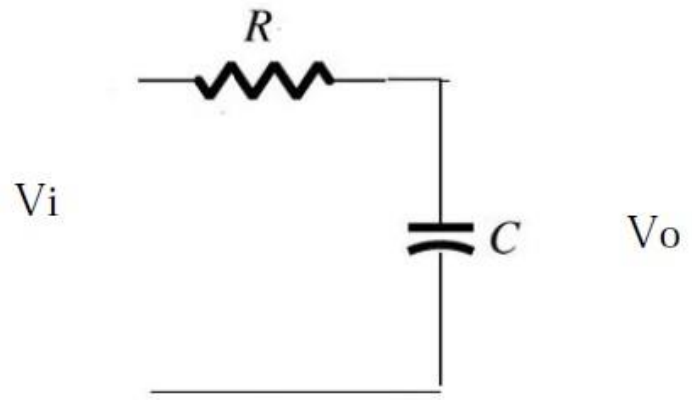
High frequency response – BJT Amplifier

At the high – frequency end, there are two factors that define the -3dB cut off point:

- ✓ The network capacitance (parasitic and introduced) and
- ✓ the frequency dependence of h_{fe} (β)

Network parameters

In the high frequency region, the RC network of the amplifier has the configuration shown below.



At increasing frequencies, the reactance X_C will decrease in magnitude, resulting in a short effect across the output and a decreased gain.

$$V_0 = \frac{V_i(-jX_C)}{R - jX_C}$$

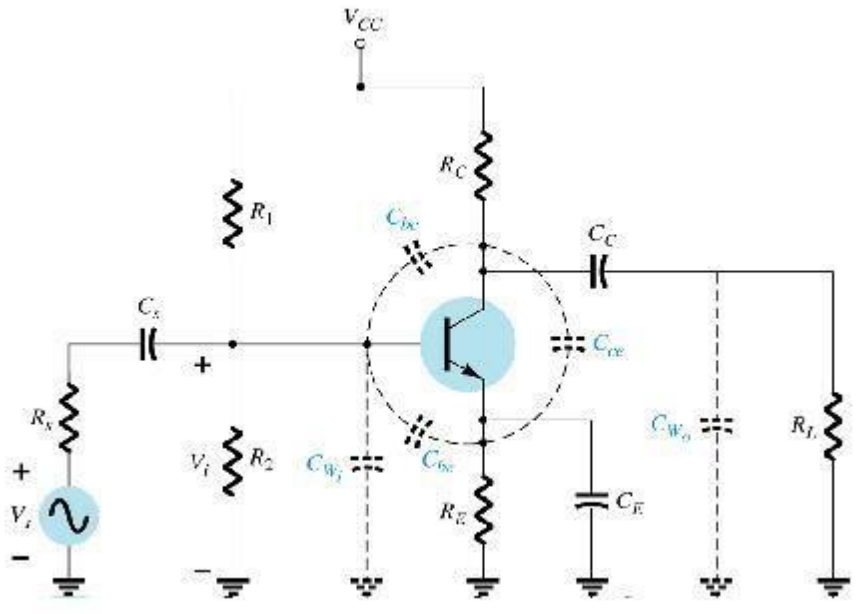
$$V_0/V_i = 1/[1 + j(R/X_C)] \; ; X_C = 1/2\pi fC$$

$$A_V = 1/[1 + j(2\pi fRC)]$$

$$\boldsymbol{A_V = 1/[1 + j(f/f_2)]}$$

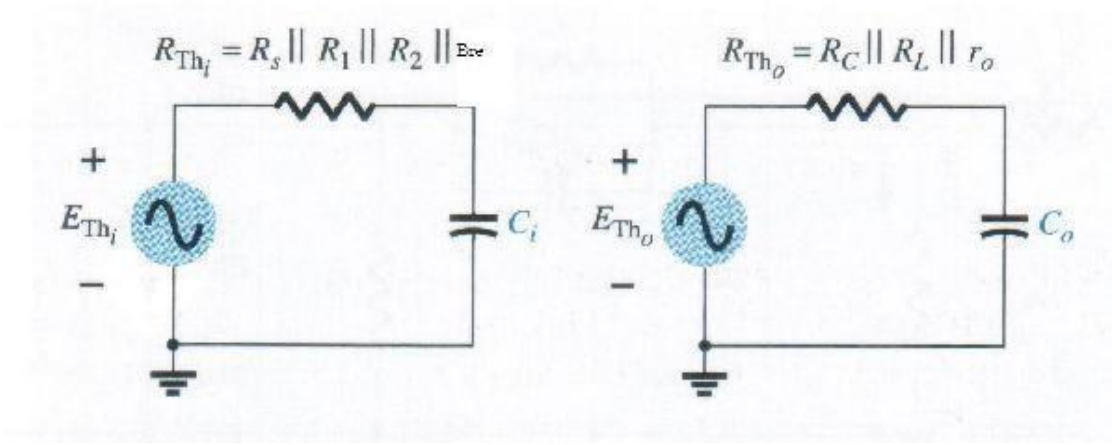
This results in a magnitude plot that drops off at 6dB / octave with increasing frequency.

Network with the capacitors that affect the high frequency response



Capacitances that will affect the high-frequency response:

- ✓ **C_{be}, C_{bc}, C_{ce}** – internal capacitances
- ✓ **C_{wi}, C_{w0}** – wiring capacitances
- ✓ **C_S, C_C** – coupling capacitors
- ✓ **C_E** – bypass capacitor



The capacitors C_S, C_C, and C_E are absent in the high frequency equivalent of the BJT amplifier. The capacitance Ci includes the input wiring capacitance, the transition capacitance Cbe, and the Miller capacitance CMi. The capacitance Co includes the output wiring capacitance Cwo, the parasitic capacitance Cce, and the output Miller capacitance CMo. In general, the capacitance Cbe is the largest of the parasitic capacitances, with Cce the smallest.

As per the equivalent circuit,

$$f_{H_i} = \frac{1}{2\pi R_{Th_i}}$$

$$R_{Thi} = R_S \| R_1 \| R_2 \| R_i$$

$$C_i = C_{wi} + C_{be} + C_{Mi} = C_{wi} + C_{be} + (1 - A_V)C_{bc}$$

At very high frequencies, the effect of C_i is to reduce the total impedance of the parallel combination of R_1, R_2, R_i, and C_i. The result is a reduced level of voltage across C_i, a reduction in I_b and the gain of the system.

For the output network,

$$f_{H_0} = \frac{1}{2\pi R_{Th_0} C_0}$$

$$R_{Th0} = R_C \parallel R_L \parallel r_0$$

$$C_0 = C_{w0} + C_{ce} + C_{M0}$$

At very high frequencies, the capacitive reactance of Co will decrease and consequently reduce the total impedance of the output parallel branches. The net result is that V_0 will also decline toward zero as the reactance X_C becomes smaller. The frequencies f_{Hi} and f_{H0} will each define a -6dB/octave asymptote. If the parasitic capacitors were the only elements to determine the high-cut off frequency, the lowest frequency would be the determining factor. However, the decrease in h_{fe} (or β) with frequency must also be considered as to whether its break frequency is lower than for f_{Hi} or f_{H0}.

h_{fe} (or β) variation

- ✓ The variation of h_{fe} (or β) with frequency will approach the following relationship

$$\boldsymbol{h_{fe} = \frac{h_{fe_{mid}}}{1 + j(f / f_\beta)}}$$

- ✓ f_β is that frequency at which h_{fe} of the transistor falls by 3dB with respect to its mid band value.

- ✓ The quantity f_β is determined by a set of parameters employed in the hybrid-π model.

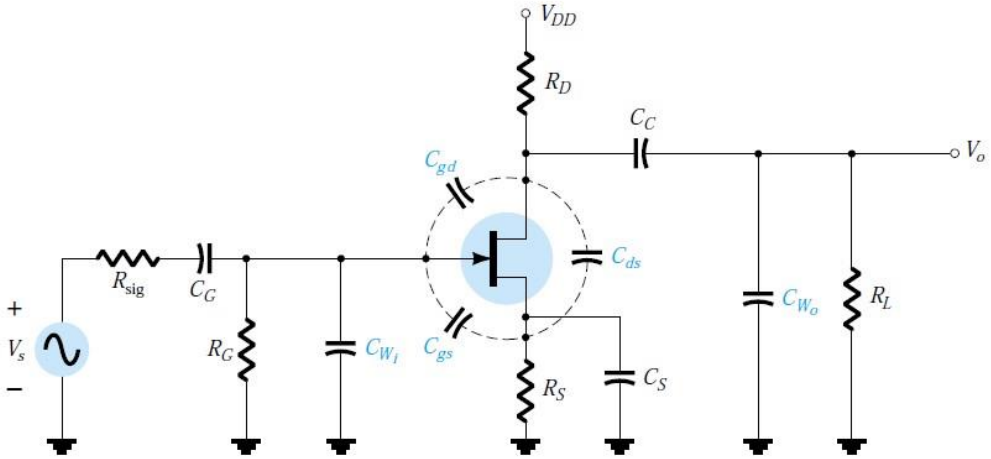
- ✓ In the hybrid-π model, r_b includes the

- ✓ base contact resistance
- ✓ base bulk resistance
- ✓ base spreading resistance

High-Frequency Response -FET Amplifier

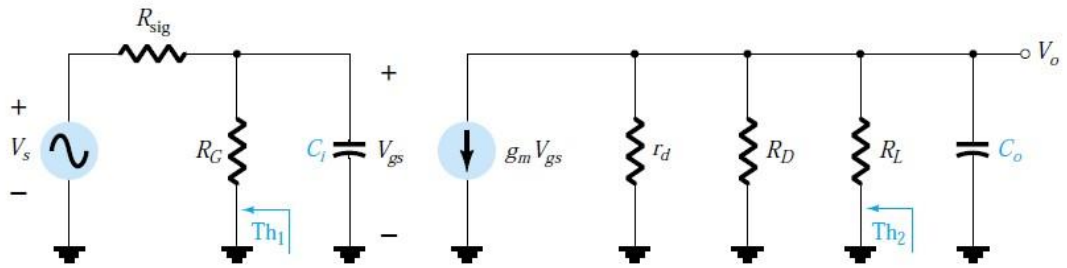
- ✓ The analysis of the high-frequency response of the FET amplifier will proceed in a very similar manner to that encountered for the BJT amplifier.

- ✓ As shown in Fig, there are inter electrode and wiring capacitances that will determine the high-frequency characteristics of the amplifier.



- ✓ The capacitors C_{gs} and C_{gd} typically vary from 1 to 10 pF, while the capacitance $C_{ds}$is usually quite a bit smaller, ranging from 0.1 to 1 pF.

- ✓ Since the network of above Fig. is an inverting amplifier, a Miller effect capacitance will appear in the high-frequency ac equivalent network appearing in following Fig.



- ✓ The cut off frequencies defined by the input and output circuits can be obtained by first finding the Thevenin equivalent circuits for each section.
- ✓ For the input circuit,

$$f_{H_i} = \frac{1}{2\pi R_{Th_1} C_i}$$

and $R_{Th1} = R_{sig} \parallel R_G$

with $C_i = C_{Wi} + C_{gs} + C_{Mi}$

and $C_{Mi} = (1 - A_V) C_{gd}$

- ✓ For the output circuit,

$$f_{H_o} = \frac{1}{2\pi R_{Th_2} C_o}$$

with $R_{Th2} = R_D \parallel R_L \parallel r_d$

and $C_0 = C_{Wo} + C_{ds} + C_{Mo}$

and $C_{M_o} = (1 - \frac{1}{A_V}) C_{gd}$

SQUARE-WAVE TESTING

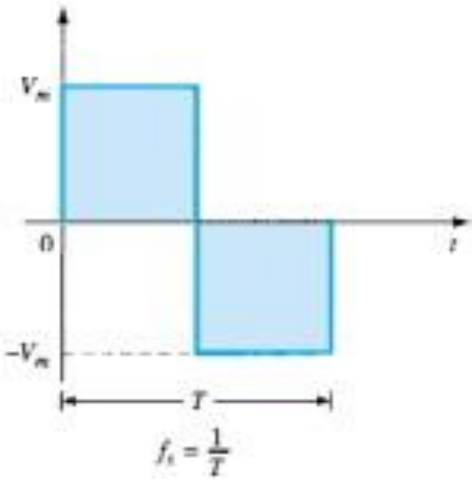
- ✓ For the frequency response of an amplifier can be determined experimentally by applying a square-wave signal to the amplifier.

- ✓ The shape of the output waveform will reveal whether the high or low frequencies are being properly amplified.

- ✓ The use of *square-wave testing* is significantly less time-consuming than applying a series of sinusoidal signals at different frequencies and magnitudes to test the frequency response of the amplifier.

- ✓ The reason for choosing a square-wave signal for the testing process is best described by examining the *Fourier series* expansion of a square wave composed of a series of sinusoidal components of different magnitudes and frequencies.

- ✓ The summation of the terms of the series will result in the original waveform.



- ✓ The Fourier series expansion for the square wave of Fig. is

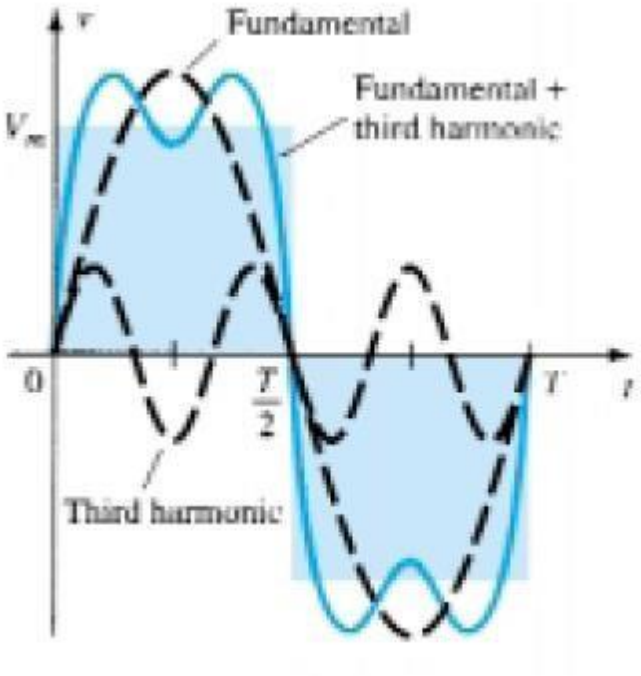
$$V = \frac{4}{\pi} V_m \left(\sin 2\pi f_s\, t + \frac{1}{3} \sin 2\pi (3 f_s)\, t + \frac{1}{5} \sin 2\pi (5 f_s)\, t + \frac{1}{7} \sin 2\pi (7 f_s)\, t + \frac{1}{9} \sin 2\pi (9 f_s)\, t + \cdots + \frac{1}{n} \sin 2\pi (n f_s)\, t \right)$$

- ✓ The first term of the series is called the *fundamental* term and in this case has the same frequency, $f_s$as the square wave.

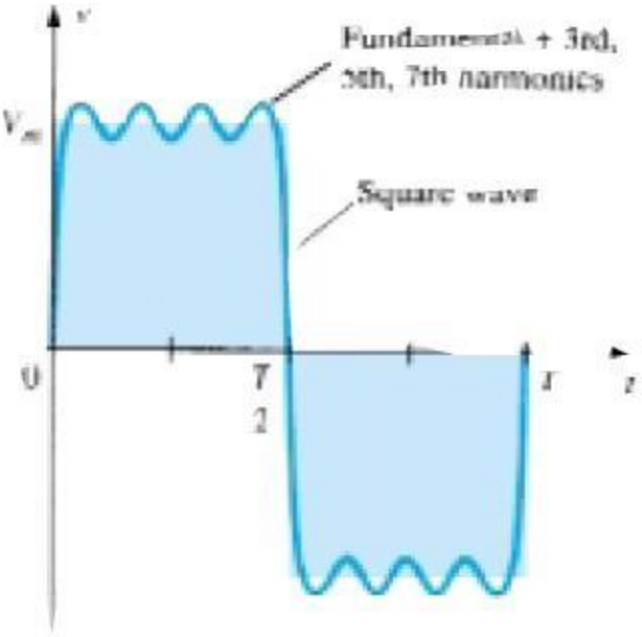
- ✓ The next term has a frequency equal to three times the fundamental and is referred to as the *third harmonic.*
- ✓ Its magnitude is one third the magnitude of the fundamental term.

- ✓ The frequencies of the succeeding terms are odd multiples of the fundamental term, and the magnitude decreases with each higher harmonic.

✓ The summation of just the fundamental term and the third harmonic in Fig. clearly results in a waveform that is beginning to take on the appearance of a square wave.

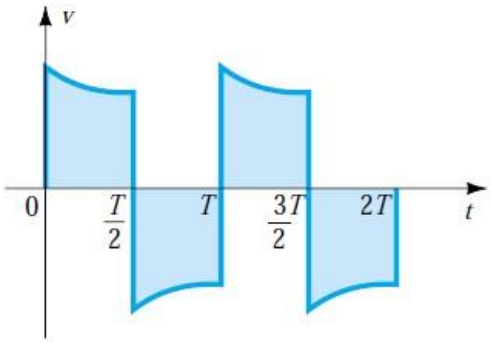


✓ Including the fifth and seventh harmonics as in Fig. takes us a step closer to the square waveform.

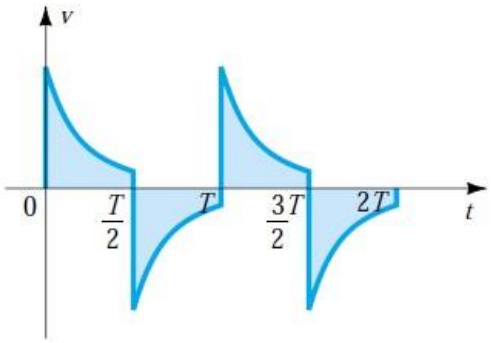


✓ Since the ninth harmonic has a magnitude greater than 10% of the fundamental term $[\frac{1}{9} \times 100\% = 11.1\%]$, the fundamental term through the ninth harmonic are the major contributors to the Fourier series expansion of the square-wave function.

- ✓ If the response is as shown in Fig. a and b, the low frequencies are not being amplified properly and the low cut off frequency has to be investigated.

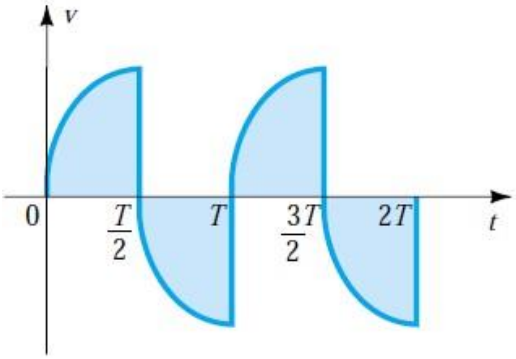


(a)

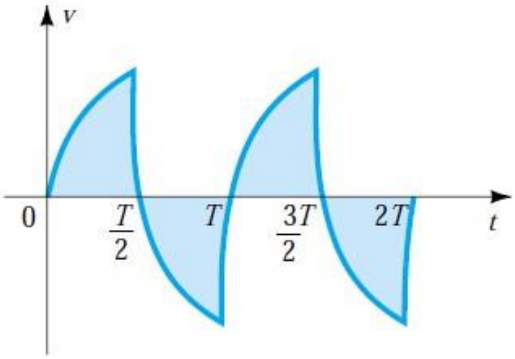


(b)

- ✓ If the waveform has the appearance of Fig. c and d, the high-frequency components are not receiving sufficient amplification and the high cut off frequency (or BW) has to be reviewed.



(c)

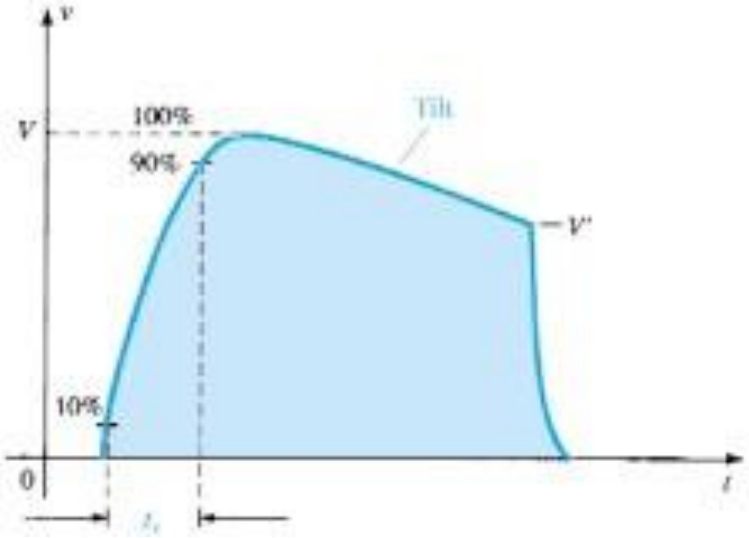


(d)

- ✓ The actual high cut off frequency (or BW) can be determined from the output waveform by carefully measuring the rise time defined between 10% and 90% of the peak value, as shown in Fig.

- ✓ The BW of the amplifier is

$$BW \cong f_{H_i} = \frac{0.35}{t_r}$$



- ✓ The low cut off frequency can be determined from the output response by carefully measuring the tilt of Fig. and substituting into one of the following equations:

$$\%\, tilt = P\% = \frac{V - V'}{V} \times 100\%$$

$$tilt = P = \frac{V - V'}{V} \text{ (Decimal form)}$$

- ✓ The low cut off frequency is then determined from

$$f_{L_0} = \frac{P}{\pi} f_S$$

Feedback and Oscillators

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References: 1. "Electronic Devices and Circuit Theory"

Robert L. Boylestad and L. Nashelsky

2. "Microelectronic Circuits"

Sedra and Smith

Feedback Amplifiers

Introduction

Most physical systems incorporate some form of feedback. It is interesting to note, though, that the theory of negative feedback has been developed by electronics engineers. In this search for methods for the design of amplifiers with stable gain for use in telephone repeaters, Harold Black, an electronics engineer with the Western Electric Company, invented the feedback amplifier in 1928. Since then the technique has been so widely used that it is almost impossible to think of electronic circuits without some form of feedback, either implicit or explicit. Furthermore, the concept of feedback and its associated theory are currently used in areas other than engineering, such as in the modelling of biological systems.

Feedback can be either **negative (degenerative)** or **positive (regenerative).** In amplifier design, negative feedback is applied to effect one or more of the following properties:

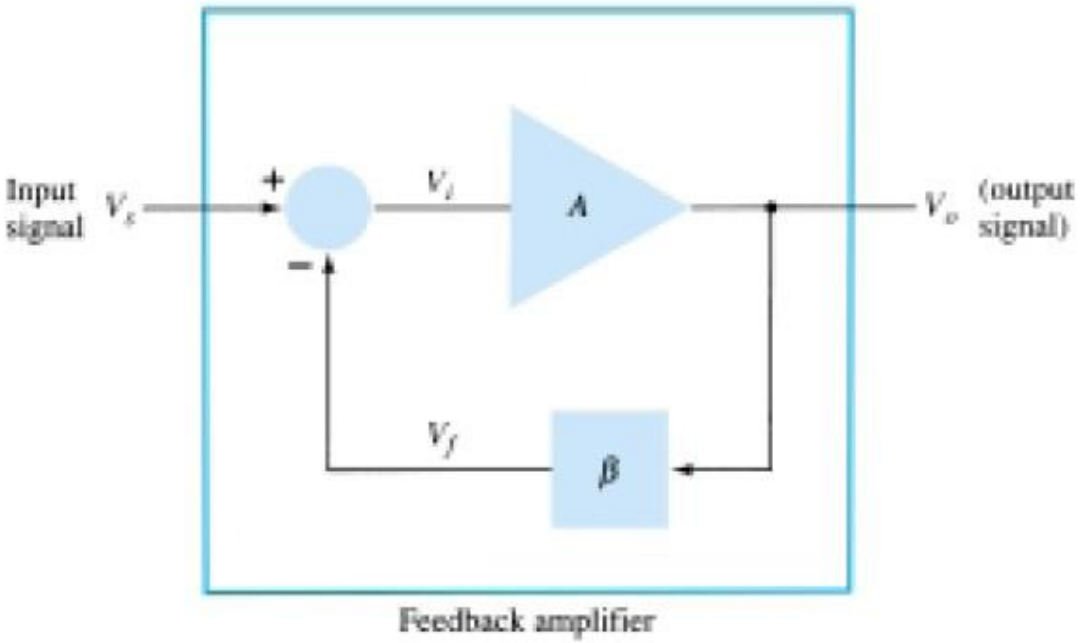
1. **Desensitize the gain**: that is, make the value of the gain less sensitive to variations in the value of circuit components, such as might he caused by changes in temperature.

2. **Reduce nonlinear distortion:** that is, make the output proportional to the input (in other words, make the gain constant, independent of signal level),

3. **Reduce the effect of noise:** that is, minimize the contribution to the output of unwanted electric signals generated, either by the circuit components themselves, or by extraneous interference.

4. **Control the input and output impedances:** that is, raise or lower the input and output impedances by the selection of an appropriate feedback topology.

5. **Extend the bandwidth of the amplifier:** All of the desirable properties are obtained at the expense of a reduction in gain. In short, the basic idea of negative feedback is trade off of gain for other desirable properties.



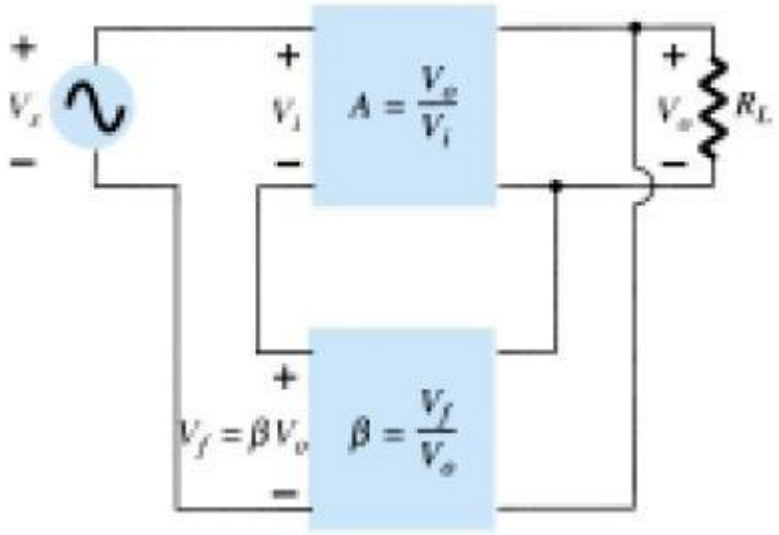
THE FOUR BASIC FEEDBACK TOPOLOGIES

Based on the quantity to be amplified (voltage or current) and on the desired form of output (voltage or current), amplifiers can be classified into four categories. In the following, we shall review this amplifier classification and point out the feedback topology appropriate in each case.

Voltage Amplifiers

Voltage amplifiers are intended to amplify an input voltage signal and provide an output voltage signal. The voltage amplifier is essentially a voltage-controlled voltage source. The input impedance is required to be high, and the output impedance is required to be low. Since the signal source is essentially a voltage source, it is convenient to represent it in terms of a Thevenin equivalent circuit. In a voltage amplifier the output quantity of interest is the output voltage. It follows that the feedback network should sample the output voltage. Also, because of the Thevenin representation of the source, the feedback signal should be a voltage that can be mixed with the source voltage in series.

A suitable feedback topology for the voltage amplifier is the **voltage-mixing voltagesampling** one shown in Fig.



Because of the series connection at the input and the parallel or shunt connection at the output, this feedback topology is also known as **series-shunt feedback.** As will be shown, this topology not only stabilizes the voltage gain but also results in a higher input resistance (intuitively, a result of the series connection at the input) and a lower output resistance (intuitively, a result **of** the parallel connection at the output), which are desirable properties for a voltage amplifier. The non inverting op-amp configuration is an example of series-shunt feedback.

Voltage gain:

Voltage gain of the amplifier

$$A = \frac{V_{out}}{V_{in}}$$

A portion of V_f of output voltage V_{out} is feedback in to the input.

Feedback ratio

$$\beta = \frac{V_f}{V_{out}}$$

$$V_{in} = V_s - V_f$$

$$= V_s - \beta V_{out}$$

$$V_{out} = AV_{in}$$

$$= A(V_s - \beta V_{out})$$

$$V_{out} = AV_s - A\beta V_{out}$$

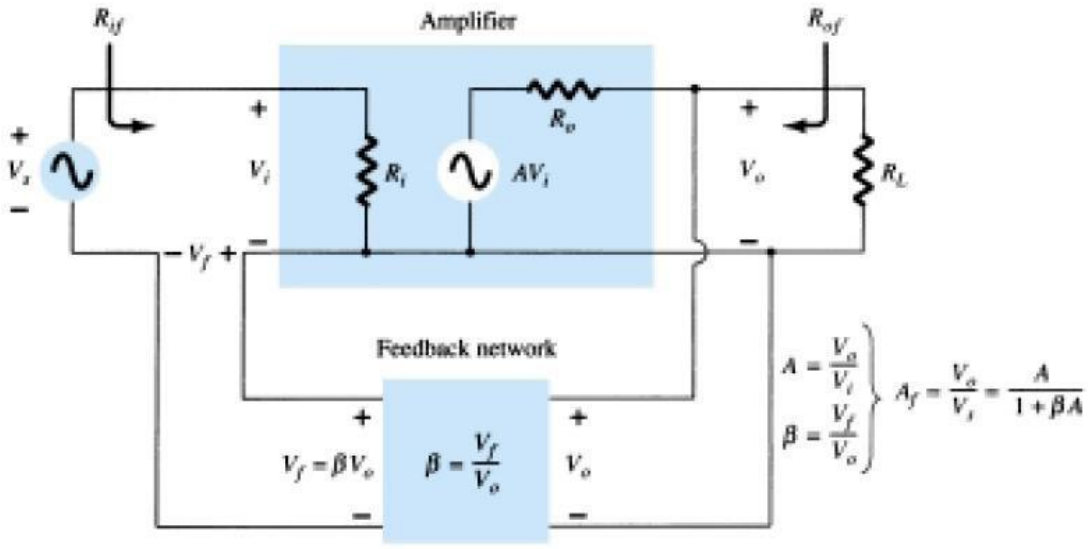
$$V_{out}(1 + A\beta) = AV_s$$

Gain with feedback,

$$A_f = \frac{V_{out}}{V_s} = \frac{A}{1 + A\beta}$$

Input Impedance with Feedback:

A more detailed voltage amplifier topology is shown in Fig.



$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta V_0}{Z_i} = \frac{V_s - \beta A V_i}{Z_i}$$

$$I_i Z_i = V_s - \beta A V_i$$

$$V_s = I_i Z_i + \beta A V_i = I_i Z_i + \beta A I_i Z_i$$

$$Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A) Z_i$$

$$Z_{if} = Z_i(1 + \beta A)$$

Output Impedance with Feedback:

The output impedance is determined by applying a voltage V, resulting in a current I, with V_s shorted out($V_s = 0$).

The voltage V is then

$$V = IZ_0 + AV_i$$

For $V_s = 0$ $V_i = -V_f$

So that $V = IZ_0 - AV_f = IZ_0 - A\beta V$

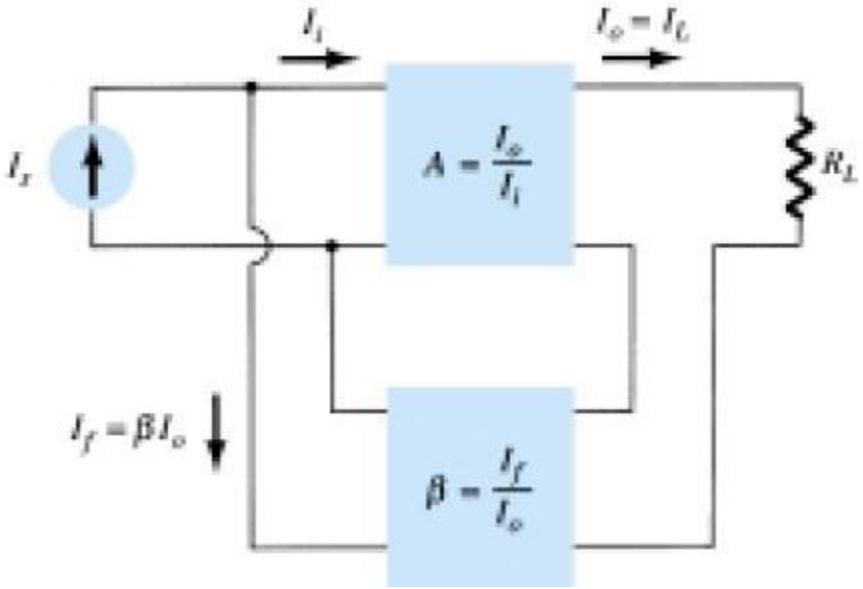
$$V + A\beta V = IZ_0$$

Output impedance with feedback,

$$Z_{of} = \frac{V}{I} = \frac{Z_0}{1 + A\beta}$$

Current Amplifiers

The input signal in a current amplifier is essentially a current, and thus the signal source is most conveniently represented by its Norton equivalent. The output quantity of interest is current; hence the feedback network should sample the output current. The feedback signal should be in current form so that it may be mixed in shunt with the source current. Thus the feedback topology suitable for a current amplifier is the **current-mixing current-sampling** topology, illustrated in Fig. Because of the Parallel (or shunt) connection at the input, and the series connection at the output, this feedback topology is also known as **shunt-series feedback.** As will be shown, this topology not only stabilizes the current gain but also results in a lower input resistance, and a higher output resistance, both desirable properties for a current amplifier.



Gain with feedback:

The gain with feedback for the network of Fig.

$$A_f = \frac{I_0}{I_s} = \frac{AI_i}{I_i + I_f} = \frac{AI_i}{I_i + \beta I_0} = \frac{AI_i}{I_i + \beta AI_i}$$

$$\boxed{A_f = \frac{A}{1 + \beta A}}$$

Input Impedance with Feedback:

$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} = \frac{V_i}{I_i + \beta I_0}$$

$$= \frac{V_i/I_i}{I_i/I_i + \beta I_0/I_i}$$

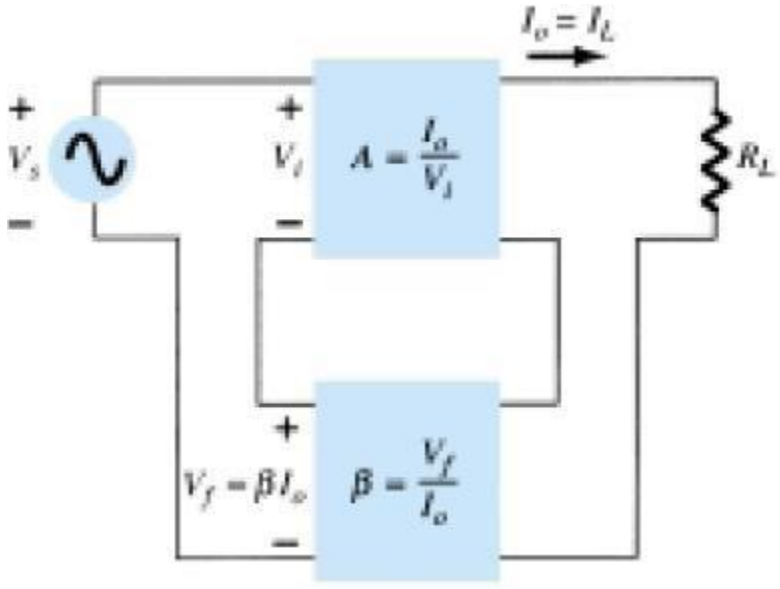
$$\boxed{Z_{if} = \frac{Z_i}{1 + \beta A}}$$

Output Impedance with Feedback:

$$\boxed{Z_{of} = Z_0(1 + \beta A)}$$

Transconductance Amplifiers

In transconductance amplifiers the input signal is a voltage and the output signal is a current. It follows that the appropriate feedback topology is the **voltage-mixing current sampling** topology, illustrated in Fig. The presence of the series connection at both the input and the output gives this feedback topology the alternative name **series series feedback.**



Gain with feedback:

The gain with feedback for the network of Fig.

$$A_f = \frac{I_0}{V_s}$$

$$V_i = V_s - V_f$$

From the network

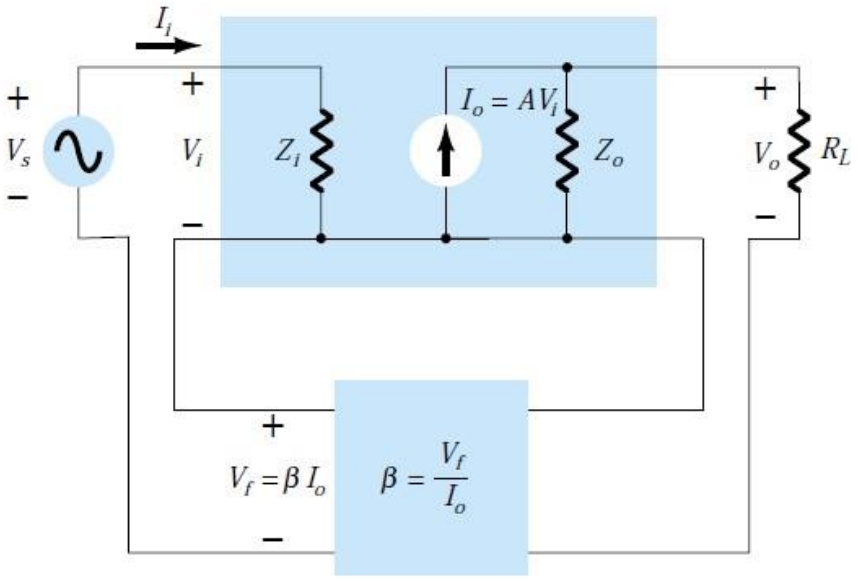
$$I_0 = AV_i = A(V_s - V_f) = A(V_s - A\beta I_0)$$

$$I_0(1 + A\beta) = AV_s$$

$$\boxed{A_f = \frac{A}{1 + A\beta}}$$

Input Impedance with Feedback:

A more detailed transconductance amplifier topology is shown in Fig.



$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta I_0}{Z_i} = \frac{V_s - \beta A V_i}{Z_i}$$

$$I_i Z_i = V_s - \beta A V_i$$

$$V_s = I_i Z_i + \beta A V_i = I_i Z_i + \beta A I_i Z_i$$

$$Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A) Z_i$$

$$Z_{if} = Z_i(1 + \beta A)$$

Output Impedance with Feedback:

The output impedance with transconductance amplifier can be determined by applying a signal V to the output with V_s shorted out, resulting in a current I, the ratio of V to I being the

output impedance. For the output part of a transconductance amplifier connection shown in Fig. 18.5, the resulting output impedance is determined as follows.

With $V_s = 0$ $\quad V_i = V_f$

$$I = \frac{V}{Z_0} - AV_i = \frac{V}{Z_0} - AV_f = \frac{V}{Z_0} - A\beta I$$

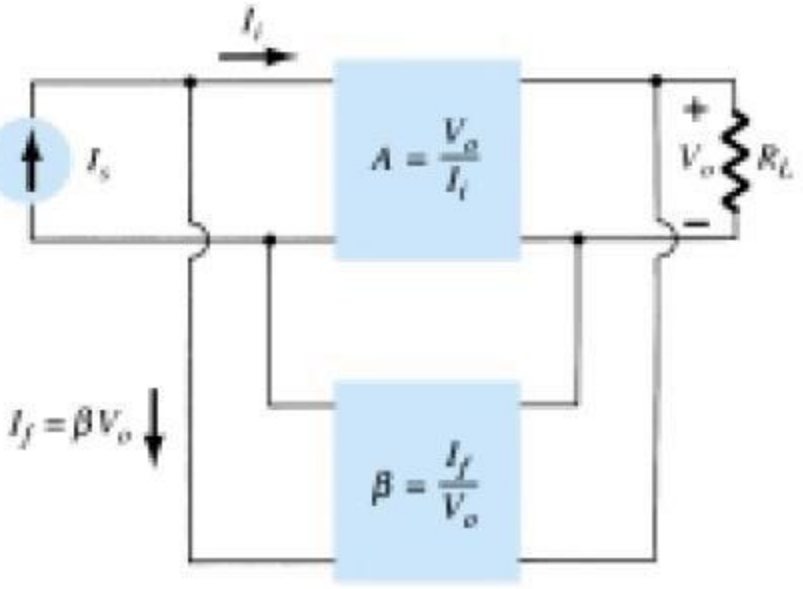
$$Z_0(1 + \beta A)I = V$$

$$\boxed{Z_{of} = Z_0(1 + \beta A)}$$

Transresistance Amplifiers

In Transresistance amplifiers the input signal is current and the output signal is voltage. It follows that the appropriate feedback topology is of the **current-mixing voltage-sampling** type, shown in Fig., The presence of the parallel (or shunt) connection at both the input and the output makes this feedback topology also known as **shunt-shunt** feedback.

An example of this feedback topology is found in the inverting op-amp configuration.



Gain with feedback:

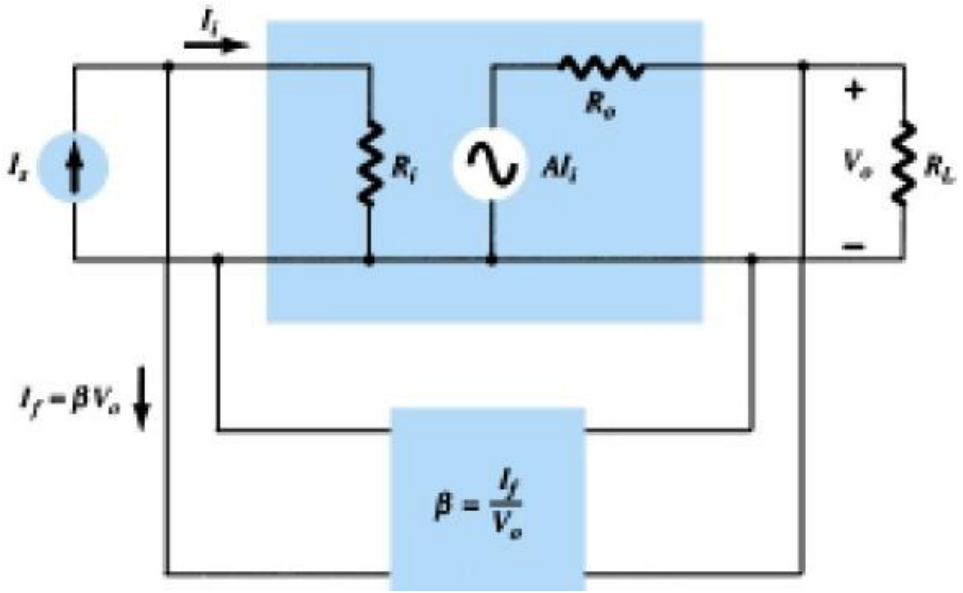
The gain with feedback for the network of Fig.

$$A_f = \frac{V_0}{I_s} = \frac{AI_i}{I_i + I_f} = \frac{AI_i}{I_i + \beta V_0} = \frac{AI_i}{I_i + \beta A I_i}$$

$$A_f = \frac{A}{1 + \beta A}$$

Input Impedance with Feedback:

A more detailed transresistance amplifier topology is shown in Fig.



$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} = \frac{V_i}{I_i + \beta V_0}$$

$$= \frac{V_i/I_i}{I_i/I_i + \beta V_0/I_i}$$

$$Z_i$$

$$Z_{if} = \frac{}{1 + \beta A}$$

Output Impedance with Feedback:

$$Z_{of} = \frac{V}{I} = \frac{Z_0}{1 + A\beta}$$

Effect of Feedback Connection on Input and Output Impedance

Impedance	Voltage Amplifier	Current Amplifier	Transconductance Amplifier	Transresistance Amplifier
Z_{if}	$Z_i(1 + \beta A)$	$\frac{Z_i}{1 + \beta A}$	$Z_i(1 + \beta A)$	$\frac{Z_i}{1 + \beta A}$
Z_{of}	$\frac{Z_0}{1 + A\beta}$	$Z_0(1 + \beta A)$	$Z_0(1 + \beta A)$	$\frac{Z_0}{1 + A\beta}$

Effect of Negative Feedback on Gain and Bandwidth

The overall gain with negative feedback is

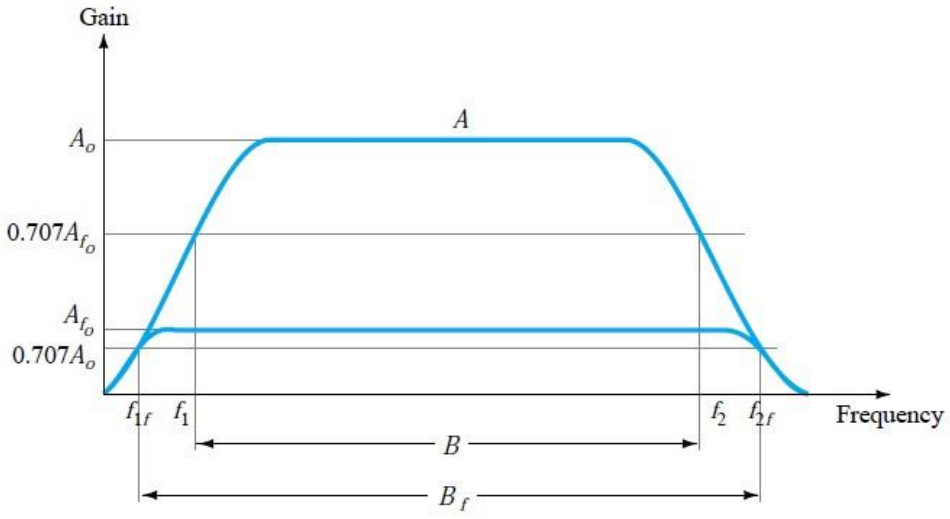
$$A_f = \frac{A}{1 + A\beta} \cong \frac{A}{A\beta} = \frac{1}{\beta} \qquad for\ \beta A \gg 1$$

As long as $\beta A \gg 1$, the overall gain is approximately $1/\beta$. We should realize that for a practical amplifier (for single low- and high-frequency breakpoints) the open-loop gain drops off at high frequencies due to the active device and circuit capacitances. Gain may also drop off at low

frequencies for capacitively coupled amplifier stages. Once the open-loop gain A drops low enough and the factor βA is no longer much larger than 1, the conclusion of Eq.

$A_f \cong 1/\beta$ no longer holds true.

Figure shows that the amplifier with negative feedback has more bandwidth (B_f) than the amplifier without feedback (*B*). The feedback amplifier has a higher upper 3-dB frequency and smaller lower 3-dB frequency.



In addition to the β factor setting a precise gain value, we are also interested in how stable the feedback amplifier is compared to an amplifier without feedback.

$$A_f = \frac{A}{1 + A\beta}$$

Differentiating the Eq. leads to

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1 + \beta A|}\left|\frac{dA}{A}\right|$$

$$\boxed{\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right| \left|\frac{dA}{A}\right|}$$

This shows that magnitude of the relative change in gain $\left|\frac{dA_f}{A_f}\right|$ is reduced by a factor $|\beta A|$ compared to that without feedback ($\left|\frac{dA}{A}\right|$).

Feedback Circuits

Voltage Amplifier:

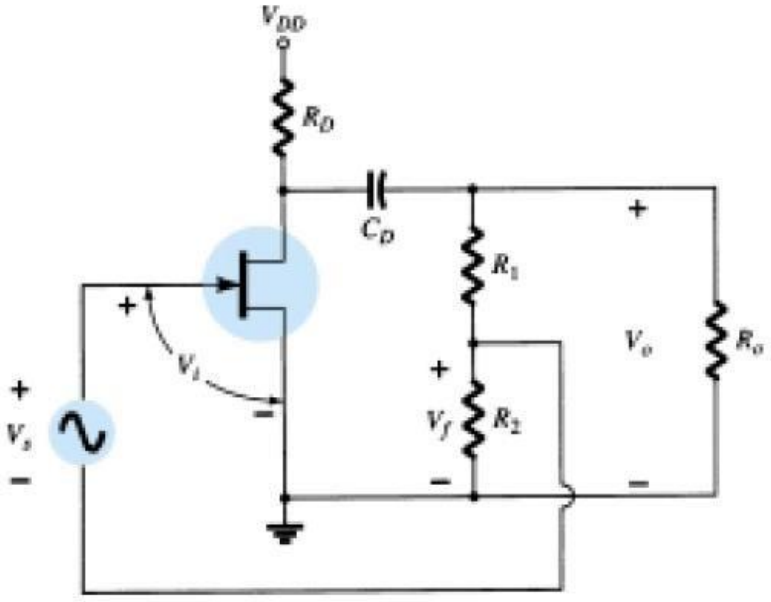
Figure shows an FET amplifier stage with Voltage Amplifier. A part of the output signal (V_0) is obtained using a feedback network of resistors R_1andR_2. The feedback voltage V_f is connected in series with the source signalV_s, their difference being the input signalV_i.

Without feedback the amplifier gain is

$$A = \frac{V_0}{V_i} = -g_m R_L$$

where $R_L$is the parallel combination of resistors

$$R_L = R_D \parallel R_0 \parallel (R_1 + R_2)$$



The feedback network provides a feedback factor of

$$\beta = \frac{V_f}{V_0} = \frac{-R_2}{R_1 + R_2}$$

Using the values of A and β above in the Eq.

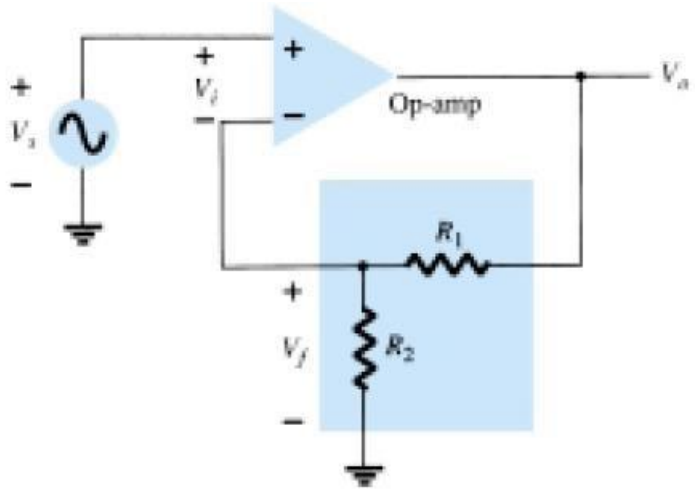
$$A_f = \frac{A}{1 + A\beta} = \frac{-g_m R_L}{1 + [\frac{R_2 R_L}{R_1 + R_2}]g_m}$$

If$A\beta \gg 1$, we have

$$A_f \cong \frac{1}{\beta} = -\frac{R_1 + R_2}{R_2}$$

Examples of Voltage Amplifier Topology

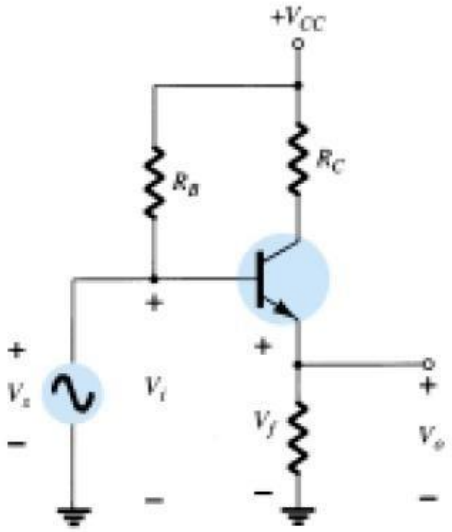
Using op-amp:



The gain of the op-amp, A, without feedback, is reduced by factor

$$\beta = \frac{R_2}{R_1 + R_2}$$

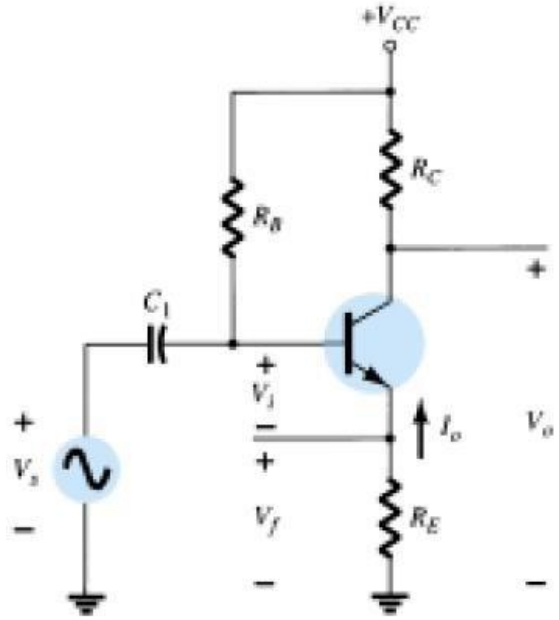
Using emitter follower:



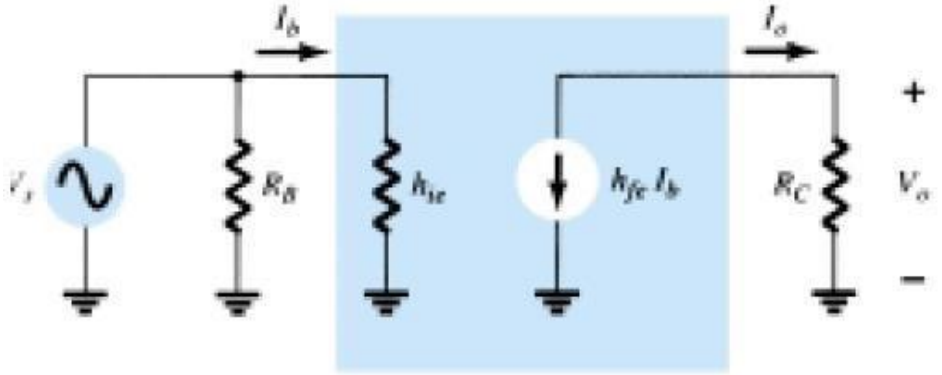
Transconductance Amplifiers:

Another feedback technique is to sample the output current (I_o) and return a proportional voltage in series with the input. While stabilizing the amplifier gain, the transconductance amplifier increases input resistance.

Figure shows a single transistor amplifier stage. Since the emitter of this stage has an unbypassed emitter, it effectively has current-series feedback. The current through resistor R_E results in a feedback voltage that opposes the source signal applied so that the output voltage V_0 is reduced. To remove the current-series feedback, the emitter resistor must be either removed or bypassed by a capacitor (as is usually done).



The ac equivalent circuit of the above Fig.



Without feedback:

$$A = \frac{I_0}{V_i} = \frac{-h_{fe}}{h_{ie} + R_E}$$

$$\beta = \frac{V_f}{I_0} = \frac{-I_0 R_E}{I_0} = -R_E$$

The input and output impedances are, respectively

$$Z_i = R_B \parallel (h_{ie} + R_E) \cong h_{ie} + R_E$$

$$Z_0 = R_c$$

With feedback:

$$A_f = \frac{I_0}{V_s} = \frac{A}{1 + A\beta} \cong \frac{-h_{fe}}{h_{ie} + h_{fe} R_E}$$

The input and output impedances are calculated as follows

$$Z_{if} = Z_i(1 + \beta A) = h_{ie} + h_{fe} R_E$$

$$Z_{0f} = Z_0(1 + \beta A)$$

$$= R_C(1 + \frac{h_{fe} R_E}{h_{ie}})$$

The voltage gain A with feedback is

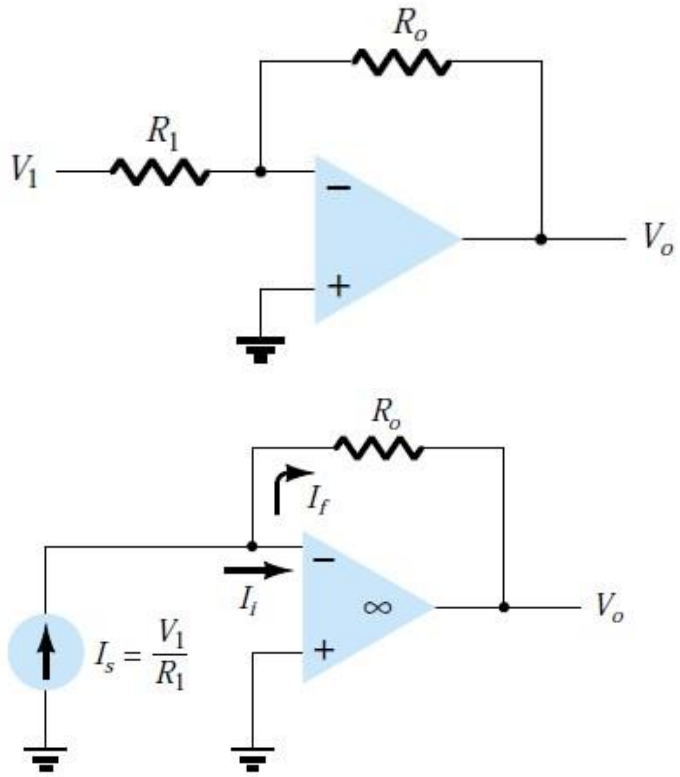
$$A_{vf} = \frac{V_0}{V_s} = \frac{I_0 R_C}{V_s} = \left(\frac{I_0}{V_s}\right) R_C = A_f R_C \cong \frac{-h_{fe} R_C}{h_{ie} + h_{fe} R_E}$$

Transresistance Amplifiers:

The constant-gain op-amp circuit of Fig. provides Transresistance amplifier. Referring to Fig. the op-amp ideal characteristics $I_i = 0$, $V_i = 0$and voltage gain of infinity, we have

$$A = \frac{V_0}{I_i} = \infty$$

$$\beta = \frac{I_f}{V_0} = \frac{-1}{R_0}$$



The gain with feedback is then

$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i} = \frac{A}{1+\beta A} = \frac{1}{\beta} = -R_0$$

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback.

$$A_{vf} = \frac{V_0}{I_s}\frac{I_s}{V_1} = (-R_0)\frac{1}{R_1} = \frac{-R_0}{R_1}$$

FEEDBACK AMPLIFIER—PHASE AND FREQUENCY CONSIDERATIONS

So far we have considered the operation of a feedback amplifier in which the feedback signal was opposite to the input signal—negative feedback. In any practical circuit this condition occurs only for some mid-frequency range of operation. We know that an amplifier gain will change with frequency, dropping off at high frequencies from the mid-frequency value. In addition, the phase shift of an amplifier will also change with frequency.

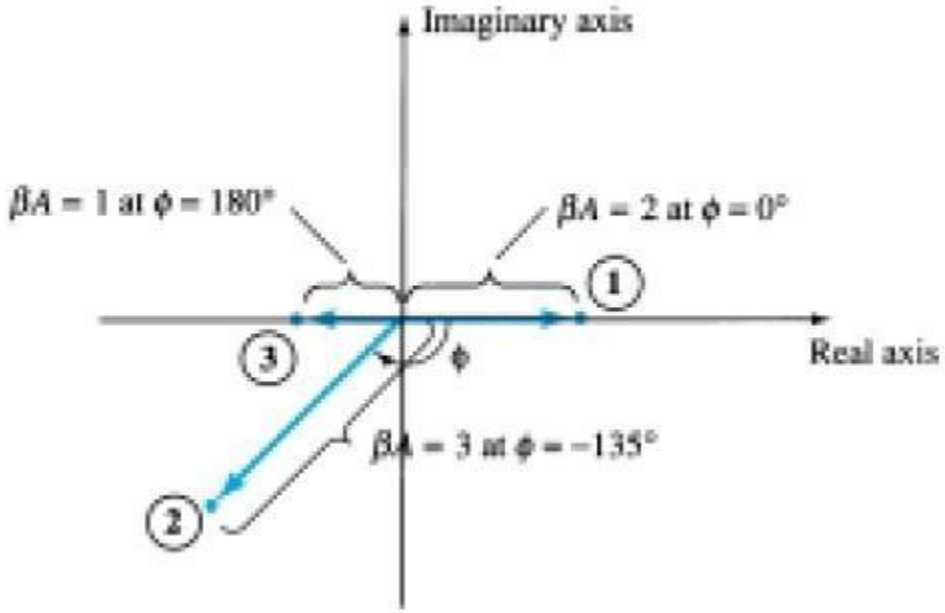
If, as the frequency increases, the phase shift changes then some of the feedback signal will add to the input signal. It is then possible for the amplifier to break into oscillations due to positive feedback. If the amplifier oscillates at some low or high frequency, it is no longer useful as an amplifier. Proper feedback-amplifier design requires that the circuit be stable at all frequencies, not merely those in the range of interest. Otherwise, a transient disturbance could cause a seemingly stable amplifier to suddenly start oscillating.

Nyquist Criterion

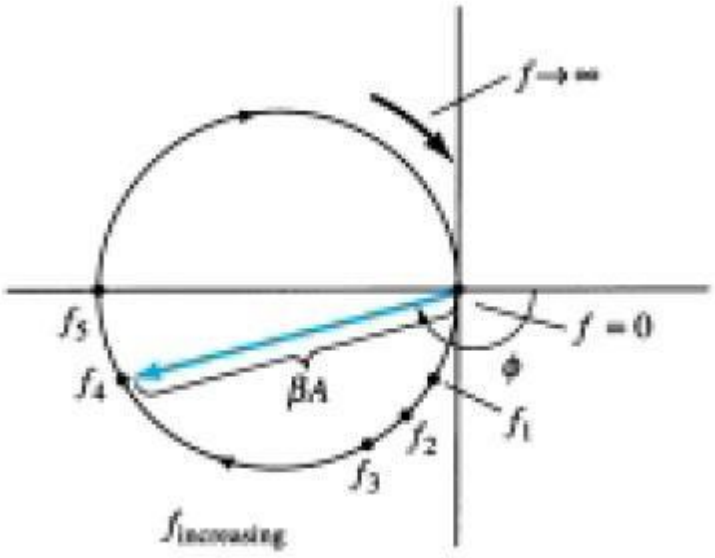
In judging the stability of a feedback amplifier, as a function of frequency, the βA product and the phase shift between input and output are the determining factors. One of the most popular techniques used to investigate stability is the Nyquist method. A

Nyquist diagram is used to plot gain and phase shift as a function of frequency on a complex plane. The Nyquist plot, in effect, combines the two Bode plots of gain versus frequency and phase shift versus frequency on a single plot. A Nyquist plot is used to quickly show whether an amplifier is stable for all frequencies and how stable the amplifier is relative to some gain or phase-shift criteria.

As a start, consider the complex plane shown in Fig.



A few points of various gain (βA) values are shown at a few different phase-shift angles. By using the positive real axis as reference (0°), a magnitude of $\beta A = 2$ is shown at a phase shift of 0° at point 1. Additionally, a magnitude of $\beta A = 3$ at a phase shift of -135° is shown at point 2 and a magnitude/phase of $\beta A = 1$ at 180° is shown at point 3. Thus points on this plot can represent *both* gain magnitude of βA and phase shift. If the points representing gain and phase shift for an amplifier circuit are plotted at increasing frequency, then a Nyquist plot is obtained as shown by the plot in Fig.

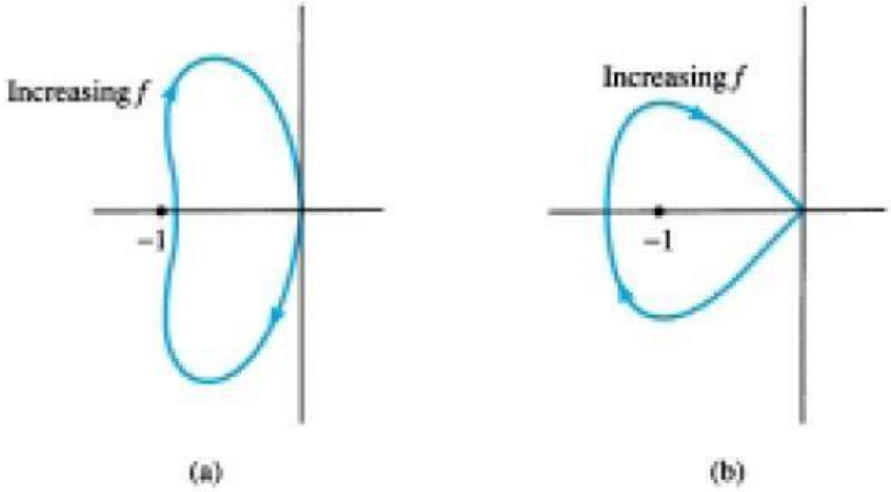


At the origin, the gain is 0 at a frequency of 0 (for *RC*-type coupling). At increasing frequency, points f_1, f_2, and f_3 and the phase shift increased, as did the magnitude of

βA. At a representative frequency f_4, the value of A is the vector length from the origin to point f_4 and the phase shift is the angle $\emptyset$. At a frequency f_5, the phase shift is 180°. At higher frequencies, the gain is shown to decrease back to 0.

The Nyquist criterion for stability can be stated as follows:

An example of the Nyquist criterion is demonstrated by the curves in Fig. The Nyquist plot in Fig. a is stable since it does not encircle the -1 point, whereas that shown in Fig. b is unstable since the curve does encircle the -1 point. Keep in mind that encircling the -1 point means that at a phase shift of 180° the loop gain (βA) is greater than 1; therefore, the feedback signal is in phase with the input and large enough to result in a larger input signal than that applied, with the result that oscillation occurs.



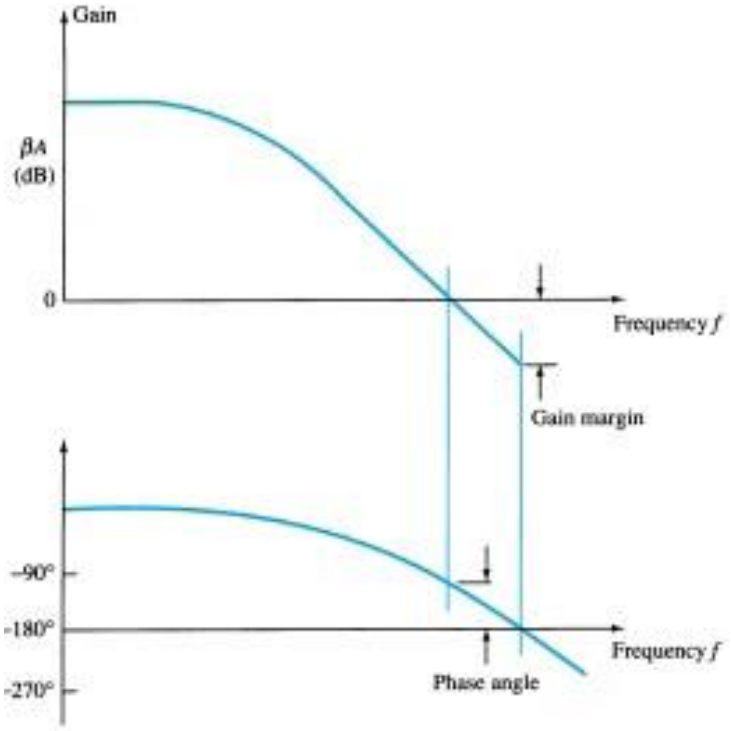
Gain and Phase Margins

From the Nyquist criterion, we know that a feedback amplifier is stable if the loop gain (βA) is less than unity (0 dB) when its phase angle is 180°. We can additionally determine some margins of stability to indicate how close to instability the amplifier is. That is, if the gain (βA) is less than unity but, say, 0.95 in value, this would not be as relatively stable as another amplifier having, say, $\beta A = 0.7$ (both measured at 180°). Of course, amplifiers with loop gains 0.95 and 0.7 are both stable, but one is closer to instability, if the loop gain increases, than the other. We can define the following terms:

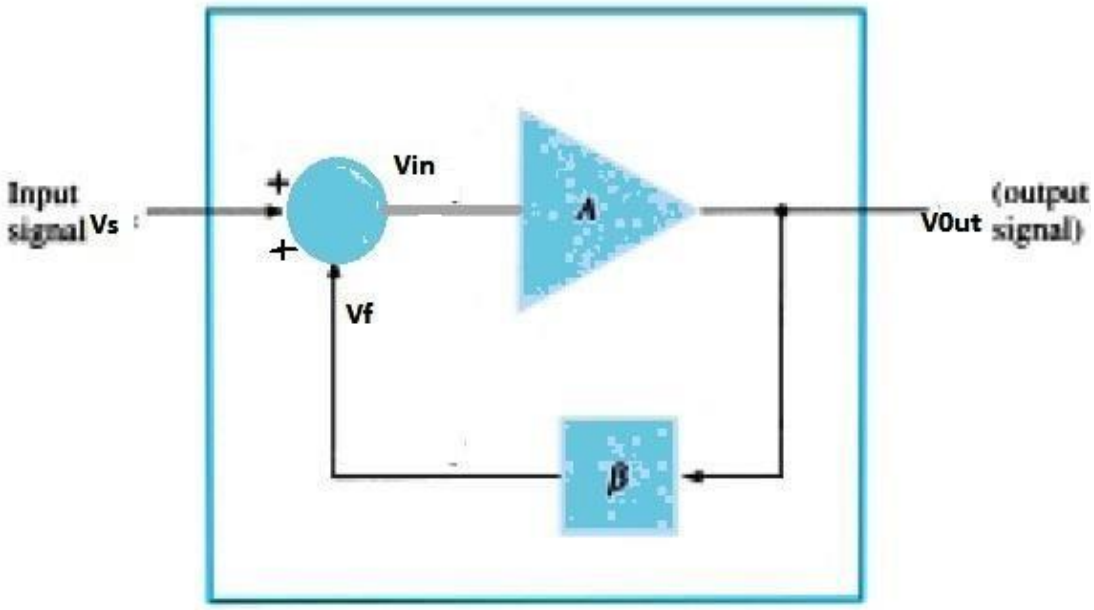
Gain margin (GM) is defined as the negative of the value of $|\beta A|$ in decibels at the frequency at which the phase angle is 180°. Thus, 0 dB, equal to a value of $\beta A = 1$, is on the border of

stability and any negative decibel value is stable. The GM may be evaluated in decibels from the curve of Fig.

Phase margin (PM) is defined as the angle of 180° minus the magnitude of the angle at which the value of $|\beta A|$ is unity (0 dB). The PM may also be evaluated directly from the curve of Fig.



Feedback Oscillator



Voltage gain of the amplifier

$$A = \frac{V_{out}}{V_{in}}$$

A portion of $V_f$of output voltage $V_{out}$is feedback in to the input. Feedback

ratio

$$\beta = \frac{V_f}{V_{out}}$$

$$V_{in} = V_s + V_f$$

$$= V_s + \beta V_{out}$$

$$V_{out} = AV_{in}$$

$$= A(V_s + \beta V_{out})$$

$$V_{out} = AV_s + A\beta V_{out}$$

$$V_{out}(1 - A\beta) = AV_s$$

Gain with feedback,

$$A_f = \frac{V_{out}}{V_s} = \frac{A}{1 - A\beta}$$

Basic operation of an Oscillator

An amplifier with positive feedback results in oscillations if the following conditions are satisfied:

(i) The loop gain (product of the gain of the amplifier and the gain of the feedback network) is unity.

(ii) The total phase shift in the loop is 0^0.

These two conditions for sustained oscillations are called Barkhausen Criteria. It is not necessary to supply an input signal to initiate oscillators. A noise voltage or transient is sufficient to initiate the oscillation.

Types of Feedback Oscillators

Feedback Oscillators are classified in to three categories.

- ✓ RC Oscillator
- ✓ LC Oscillator
- ✓ Crystal Oscillator

RC Oscillator

RC Oscillator may be of one of the two following forms.

- ✓ Wien's Bridge Oscillator
- ✓ Phase Shift Oscillator

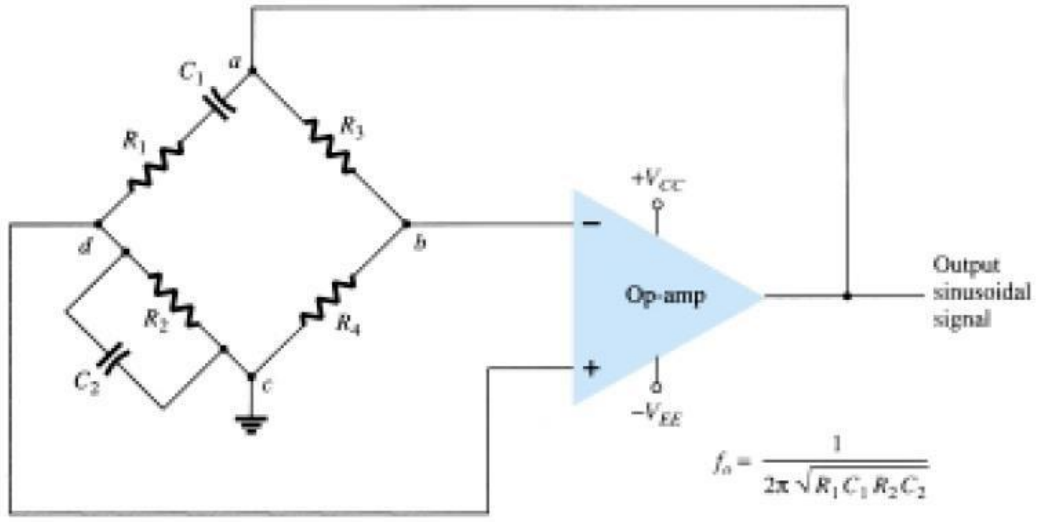
Wien's Bridge Oscillator

- ✓ The Wien's Bridge Oscillator has become standard circuit for variable frequency test circuits in the audio frequency range.

- ✓ The Oscillator is simple and stable in operation.

- ✓ The instruments always produce a sine-wave signal, variable in both amplitude and frequency and usually provide a square wave output as well.

- ✓ The maximum amplitude of the output waveform is typically in the order of 25V whereas the range of frequency covers at least radio frequency range from 20Hz to 20 KHz.



- ✓ When the bridge is balanced and Neglecting loading effects of the op-amp input and output impedances, the analysis of the bridge circuit results in

$$\frac{R_2}{R_1} = \frac{R_3}{R_4} + \frac{C_2}{C_1}$$

$$f_0 = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

- ✓ If, in particular, the values are $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the resulting oscillator frequency is

$$f_0 = \frac{1}{2\pi RC}$$

$$\frac{R_3}{R_4} = 2$$

- ✓ Thus a ratio of R_3 to R_4 greater than 2 will provide sufficient loop gain for the circuit to oscillate at the frequency.

Phase Shift Oscillator

- ✓ When an audio frequency (AF) Oscillator is to be used over a comparatively a limited frequency range, simplified RC networks are usually employed.

- ✓ A phase shift Oscillator which can be used for generation of sinusoidal voltages up to a frequency range of several hundred KHz.

- ✓ The circuit consists of an amplifier stage, followed by three cascaded arrangements of resistor R and capacitor C to provide necessary positive feedback.

- ✓ The amplifier shifts the phase of any voltage by 180^0.

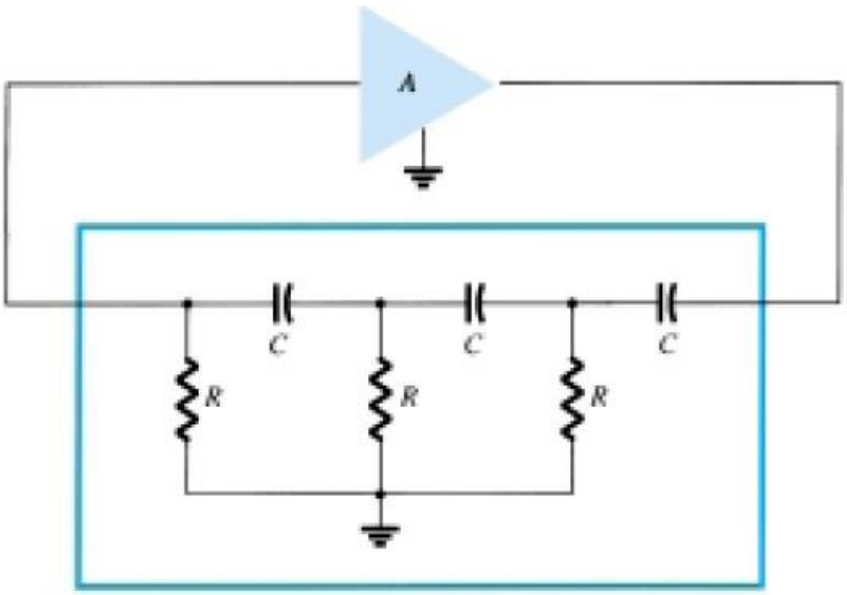
- ✓ The RC network is necessary to provide an additional phase shift of exactly 180^0 .

- ✓ This additional phase shift is obtained from the RC network only at a specific frequency.

- ✓ Thus a feedback voltage is in phase with the voltage input to the amplifier at that frequency.

- ✓ The phase shift network for the phase-shift Oscillator consists of equal valued capacitors and resistors connected in cascade.

- ✓ Each stage provides a phase shift $60^0$with the total phase shift being180^0.



Feedback network

- ✓ Using classical network analysis, we find that

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

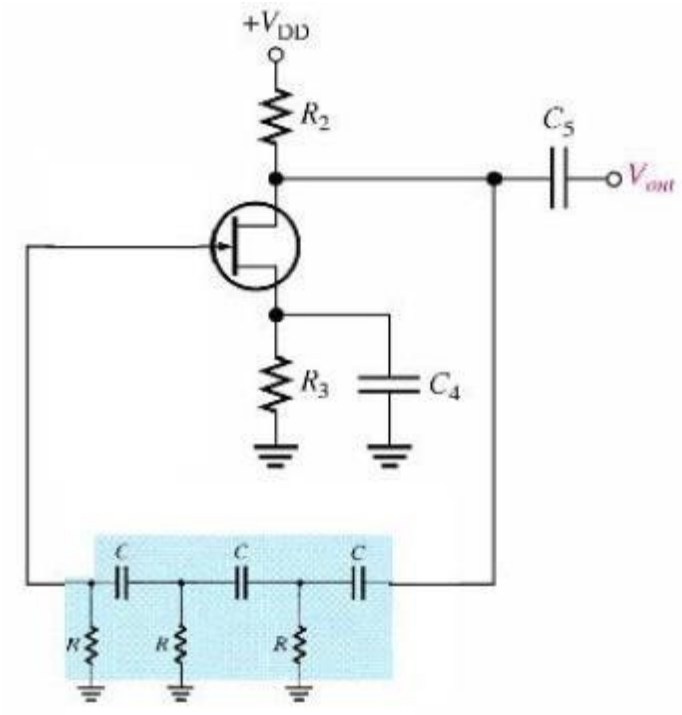
$$\boxed{\beta = 29}$$

and the phase shift is 180^0.

- ✓ For the loop gain βA to be greater than unity, the gain of the amplifier stage must be greater than $1/\beta$or 29:

$$A > 29$$

FET phase shift oscillator



- ✓ The amplifier stage is self biased with a capacitor bypassed source resistor R_S and a drain bias resistor R_D. The FET device parameters of interest are $g_m$andr_d.

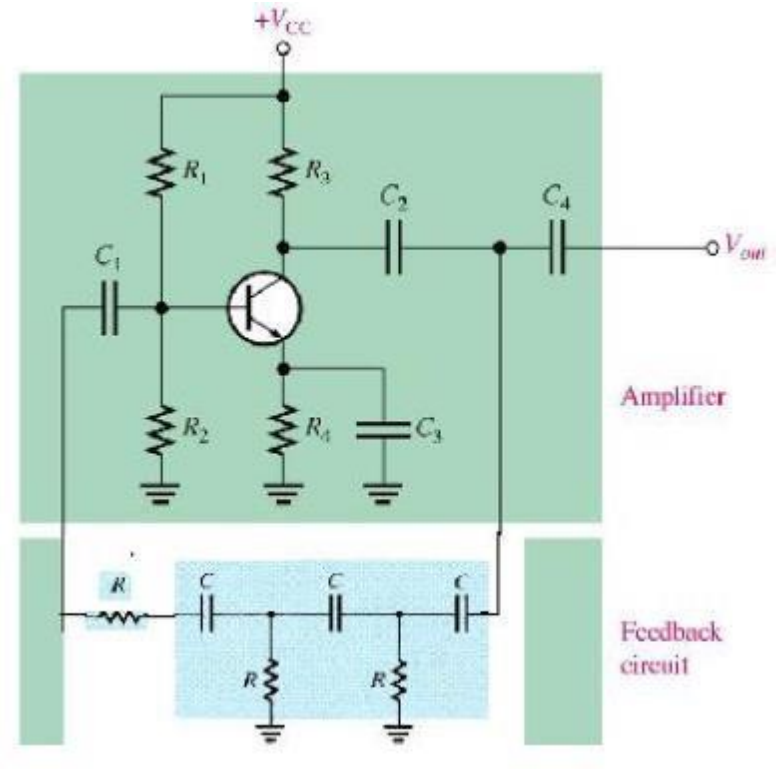
- ✓ $|A| = g_m R_L \; where \; R_L = (R_D r_d / R_D + r_d)$

- ✓ At the operating frequency, we can assume that the input impedance of the amplifier is infinite**.**

- ✓ This is a valid approximation provided; the oscillator operating frequency is low enough so that FET capacitive impedances can be neglected.

- ✓ The output impedance of the amplifier stage given by R_L should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs.

RC Phase shift Oscillator - BJT version



- ✓ If a transistor is used as the active element of the amplifier stage, the output of the feedback network is loaded appreciably by the relatively low input resistance (h_{ie}) of the transistor.

- ✓ An emitter-follower input stage followed by a common emitter amplifier stage could be used. If a single transistor stage is desired, the use of voltage-shunt feedback is more suitable. Here, the feedback signal is coupled through the feedback resistor R' in series with the amplifier stage input resistance (R_i).

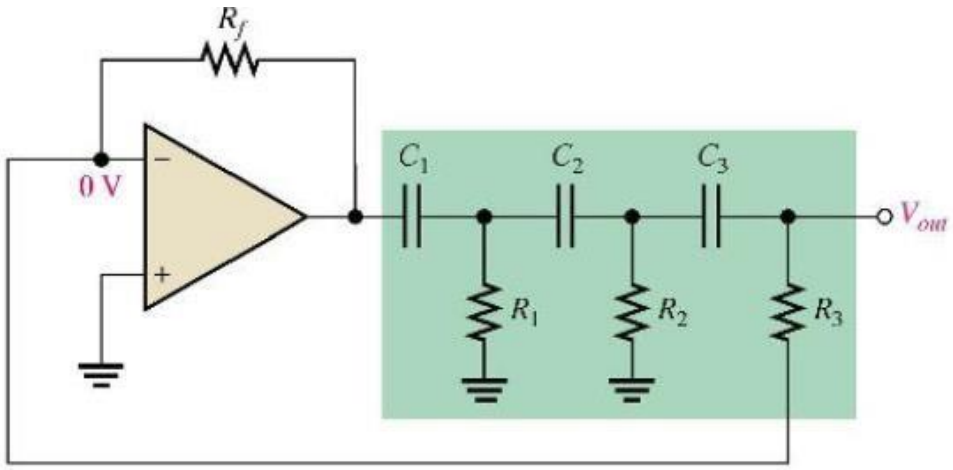
$$f = \frac{1}{2\pi RC}\frac{1}{\sqrt{6 + 4(R_C/R)}}$$

- ✓ For the loop gain to be greater than unity, the requirement on the current gain of the transistor is found to be

$$h_{fe} > 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

IC phase shift Oscillator

✓ As IC circuits have become more popular, they have been adapted to operate in oscillator circuits.



Crystal Oscillator

✓ A Crystal Oscillator is basically a tuned circuit Oscillator using a piezoelectric crystal as a resonant circuit.

✓ The crystal (usually quartz) has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate.

✓ Crystal Oscillators are used whenever great stability is required, such as communication transmitters and receivers.

Characteristics of a Quartz Crystal

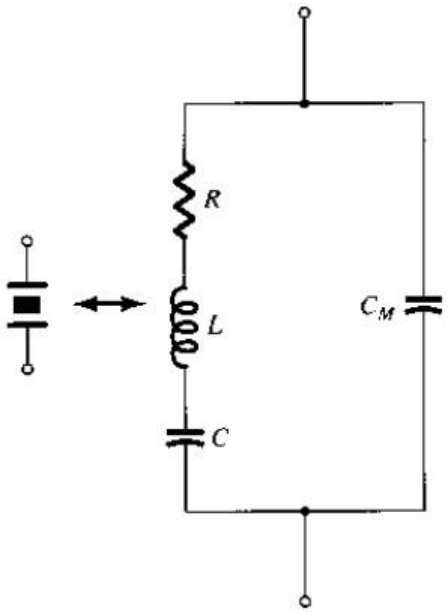
✓ A quartz crystal exhibits the property that when mechanical stress is applied across one set of its faces, a difference of potential develops across the opposite faces.

- ✓ This property of a Crystal is called ‘Piezoelectric effect’.

- ✓ Similarly, a voltage applied across one set of faces of the Crystal causes mechanical distortion in the Crystal shape.

- ✓ When alternating voltage is applied to a crystal, mechanical vibrations are set up these vibrations having a natural resonant frequency dependent on the Crystal.

- ✓ Although the Crystal has electromechanical resonance, we can represent the Crystal action by equivalent electrical circuit as shown.



- ✓ The inductor L and the capacitor C represent electrical equivalents of Crystal mass and compliance respectively, whereas resistance R is an electrical equivalent of the crystal structures internal friction.

- ✓ The shunt capacitance C_M represents the capacitance due to mechanical mounting of the crystal.

- ✓ Because the crystal losses, represented by R, are small, the equivalent crystal Q factor is high – typically 20,000.

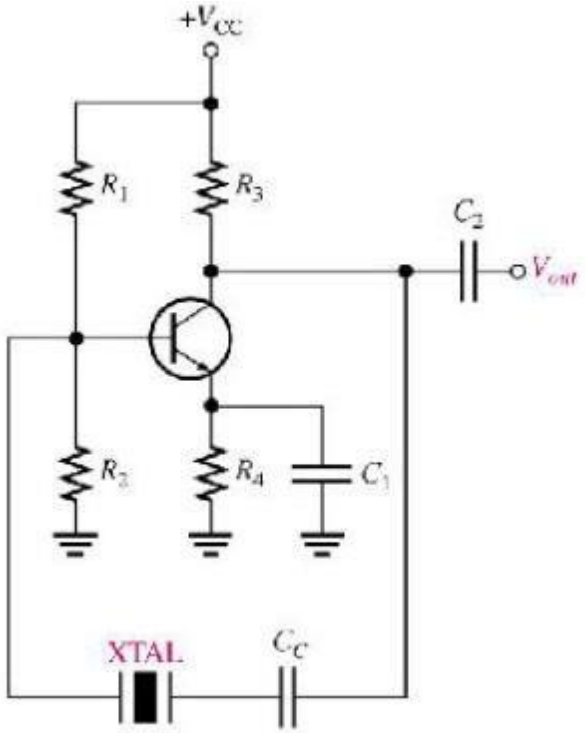
- ✓ Values of Q up to almost 10^6 can be achieved by using Crystals.

- ✓ The Crystal can have two resonant frequencies.

Series resonant circuits

- ✓ To excite a crystal for operation in the series-resonant mode, it may be connected as a series element in a feedback path.

- ✓ At the series resonant frequency of the crystal, its impedance is smallest and the amount of feedback is largest.



- ✓ R_3 can be replaced with RF choke. ResistorsR_1, R_2 and R_E provide a voltage divider stabililized dc bias circuit.

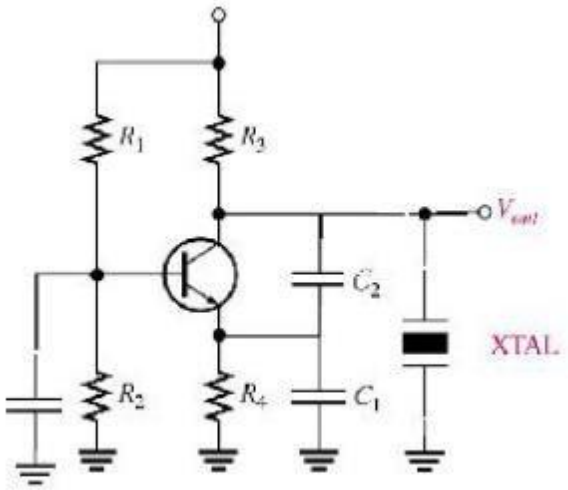
- ✓ Capacitor C_E provides ac bypass of the emitter resistor, RFC coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal.

- ✓ The voltage feedback from collector to base is a maximum when the crystal impedance is minimum (in series – resonant mode).

- ✓ The resulting circuit frequency of oscillation is set by the series – resonant frequency of the crystal.

- ✓ The circuit frequency stability is set by the crystal frequency stability which is good.

Parallel resonant circuits



- ✓ Since the parallel resonant impedance of a crystal is a maximum value, it is connected in shunt.

- ✓ Maximum voltage is developed across the crystal at its parallel resonant frequency.

- ✓ The voltage is coupled to the emitter by a capacitor voltage divider capacitors C_1 andC_2.

Operational Amplifier

Prepared by:

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Assistant Professor

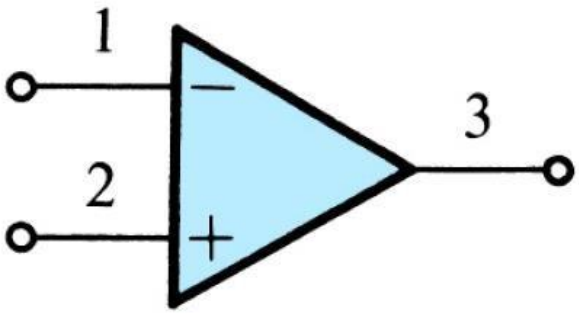
Department of Electrical Engineering

GCE, Keonjhar

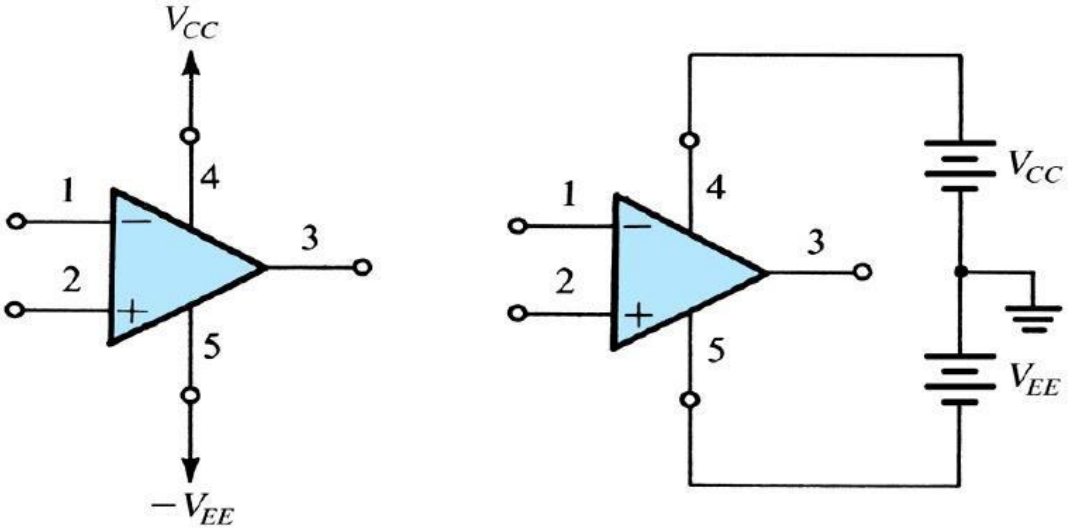
Reference: "Microelectronic Circuits"

Sedra and Smith Operational Amplifier

- ✓ An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance.
- ✓ Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits.
- ✓ An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.
- ✓ An op-amp is designed to perform mathematical operations like addition, substruction, multiplication, division, differentiation, integration etc.
- ✓ The op amp has three terminals: two input terminals and one output terminal.
- ✓ Figure shows the symbol to represent the op amp. Terminals 1 and 2 are input terminals, and terminal 3 is the output terminal.



- ✓ Most IC op amps require two dc power supplies, as shown in Fig. Two terminals, 4 and 5, are brought out of the op-amp package and connected to a positive voltage $V_{CC}$and a negative voltage$-V_{EE}$, respectively.



Function and Characteristics of the Ideal Op Amp

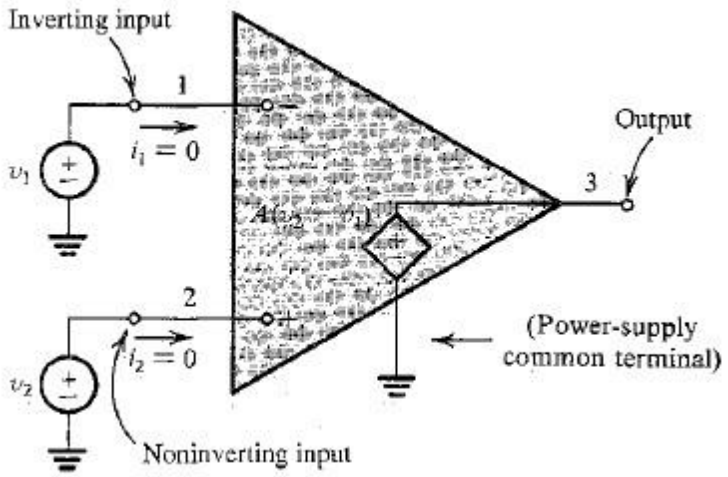
- ✓ The op amp is designed to sense the difference between the voltage signals applied at its two input terminals (i.e., the quantity$v_2 - v_1$), multiply this by a number A, and cause the resulting voltage $A(v_2 - v_1)$ appear at output terminal 3.

- ✓ The voltage $v_1$means the voltage applied between terminal 1 and ground.

- ✓ The ideal op amp is not supposed to draw any input current; that is, the signal current into terminal 1 and the signal current into terminal 2 are both zero. In other words, the input impedance of an ideal op amp is supposed to be infinite.

- ✓ The voltage between terminal 3 and ground will always be equal to$A(v_2 - v_1)$, independent of the current that may be drawn from terminal 3 into load impedance. In other words, the output impedance of an ideal op amp is supposed to be zero.

- ✓ Putting together all of the above, we arrive at the equivalent circuit model shown in Fig.



- ✓ Note that the output is in phase with (has the same sign as) v_1 and is out of phase with (has the opposite sign of)v_2. For this reason, input terminal 1 is called the **inverting input terminal** and is distinguished by a " - " sign, while input terminal 2 is called the **non inverting input terminal** and is distinguished by a "+" sign.

- ✓ The op amp responds only to the difference signal$(v_2 - v_1)$, *and* hence ignores any signal common to both inputs. That is, if$v_1 = v_2 = 1V$, then the output will ideally be zero. We call this property **common-mode rejection,** and we conclude that an ideal op amp has zero common-mode gain or, equivalently, infinite common-mode rejection.

- ✓ An important characteristic of op amps is that they are **direct-coupled** or **dc amplifiers.**

- ✓ The ideal op amp has a gain A that remains constant down to zero frequency and up to infinite frequency. That is, ideal op amps will amplify signals of any frequency with equal gain, and are thus said to have infinite bandwidth.

- ✓ The ideal op amp has a gain A whose value is very large and ideally infinite.

In summary, characteristics of ideal op amp are

1. Infinite input impedance
2. Zero output impedance
3. Zero common mode gain or infinite common mode rejection
4. Infinite open-loop gain A
5. Infinite band width

Differential and Common-Mode signals

The difference between two input signals gives the differential input, v_{Id} and the average of the two input signals gives the common mode input, v_{Icm} as given below:

$$v_{Id} = v_2 - v_1$$

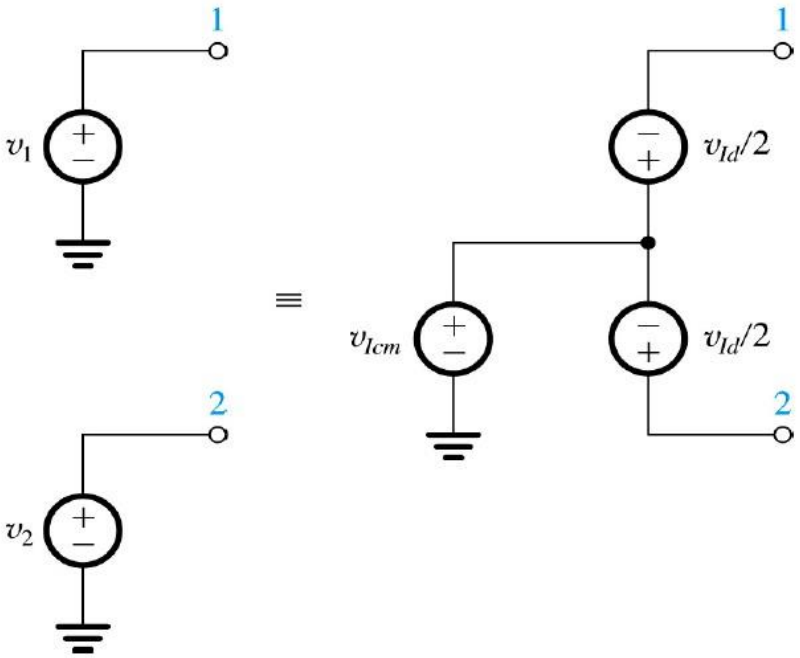
$$v_{Icm} = \frac{1}{2}(v_1 + v_2)$$

Expressing inputs in terms of differential and common mode gains, we get

$$v_1 = v_{Icm} - v_{Id}/2$$

$$v_2 = v_{Icm} + v_{Id}/2$$

These equations can in turn lead to the pictorial representation in Fig.

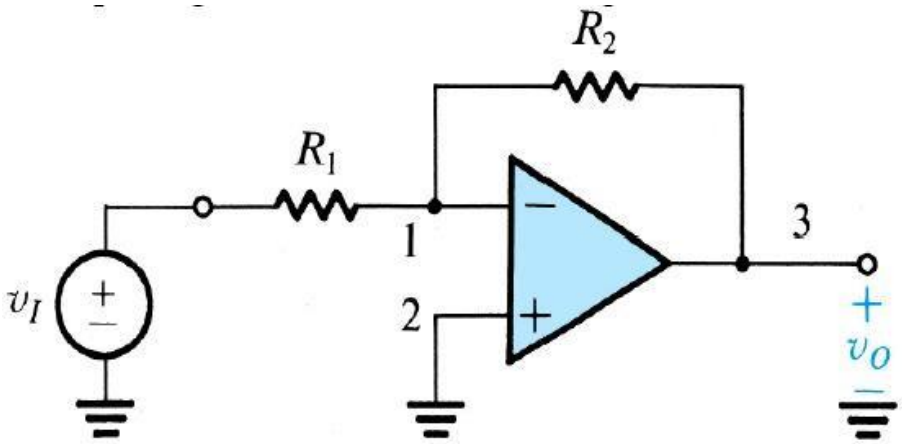


Basic Op amp Configurations

Op amps are not used alone; rather, the op amp is connected to passive components in a feedback circuit. There are two such basic circuit configurations employing an op amp and two resistors: The inverting configuration, and the non-inverting configuration.

The Inverting Configuration

Inverting Configuration consists of one op amp and two resistors R_1 andR_2. Resistor R_2 is connected from the output terminal of the op amp, terminal 3, back to the inverting or negative input terminal, terminal 1, as applying **negative feed-back;** if R_2 were connected between terminals 3 and 2 we would have called this **positive feed-back.** In addition to addingR_2, we have grounded terminal 2 and connected a resistor between terminal 1 and an input signal source with a voltagev_I.



The output of the overall circuit is taken at terminal 3 (i.e., between terminal 3 and ground). Terminal 3 is, of course, a convenient point to take the output, since the impedance level there is ideally zero. Thus the voltage v_0 will not depend on the value of the current that might be supplied to load impedance connected between terminal 3 and ground.

The Closed-Loop Gain

Analyzing the circuit in Fig. to determine the **closed-loop gain *G,*** defined as

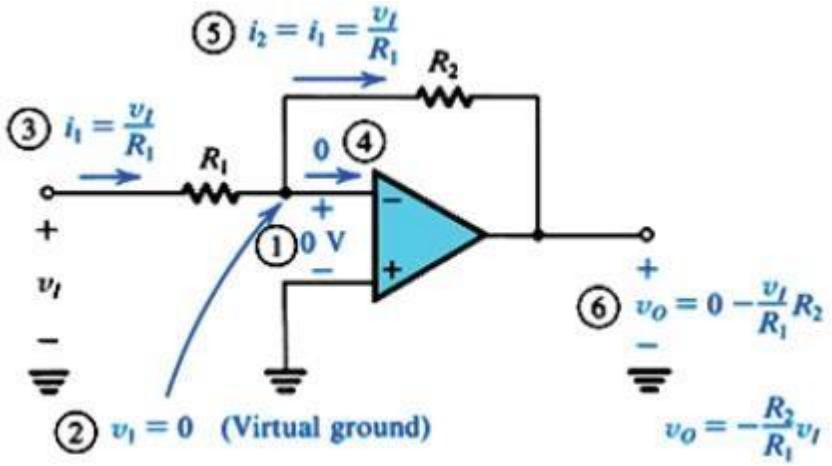
$$G = \frac{v_0}{v_I}$$

We will do so assuming the op amp to be ideal. The gain A is very large (ideally infinite). If we assume that the circuit is "working" and producing a finite output voltage at terminal 3, then the voltage between the op amp input terminals should be negligibly small and ideally zero.

$$v_2 - v_1 = \frac{v_0}{A} = 0$$

It follows that the voltage at the inverting input terminal is given by $v_1 = v_2$.That is, because the gain A approaches infinity, the voltage v_1 approaches and ideally equalsv_2. We speak of this as the two input terminals "tracking each other in potential." We also speak of a "virtual short circuit" that exists between the two input terminals. Here the word *virtual* should be emphasized, and one should *not* make the mistake of physically shorting terminals 1 and 2 together while analyzing a circuit. A **virtual short circuit** means that whatever voltage is at 2 will automatically appear at 1 because of the infinite gain A, But terminal 2 happens to be connected to ground; thus, $v_2 = 0$ and $v_1 = 0$. We speak of terminal 1 as being a **virtual ground—**that is, having zero voltage but not physically connected to ground.

Applying Ohm's law to find the currenti_1 throughR_1, (see Fig.) as follows, we get



$$i_1 = \frac{v_I - v_1}{R_1} == \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

This current cannot go into the op amp, since the ideal op amp has infinite input impedance and hence draws zero current. It follows that i_1 will have to flow through R_2 to the lowimpedance terminal 3. We can then apply Ohm's law to $R_2$and determinev_0; that is,

$$v_0 = v_1 - i_1 R_2$$

$$v_0 = 0 - \frac{v_I}{R_1} R_2$$

$$\frac{v_0}{v_I} = -\frac{R_2}{R_1}$$

The closed-loop gain is simply the ratio of the two resistances R_2andR_1 . The minus sign means that the closed-loop amplifier provides signal inversion. Thus if $R^2/R_1 = 10$ and we apply at the input a sine-wave signal of 1V peak-to-peak, then the output will be a sine wave of 10V peak-to-peak and phase-shifted 180° with respect to the input sine wave. Because of the minus sign associated with the closed-loop gain, this configuration is called the **inverting configuration.**

Note

i. Since the closed-loop gain depends entirely on external passive components (resistors R_1andR_2), we can make the closed-loop gain as accurate as we want by selecting passive components of appropriate accuracy.

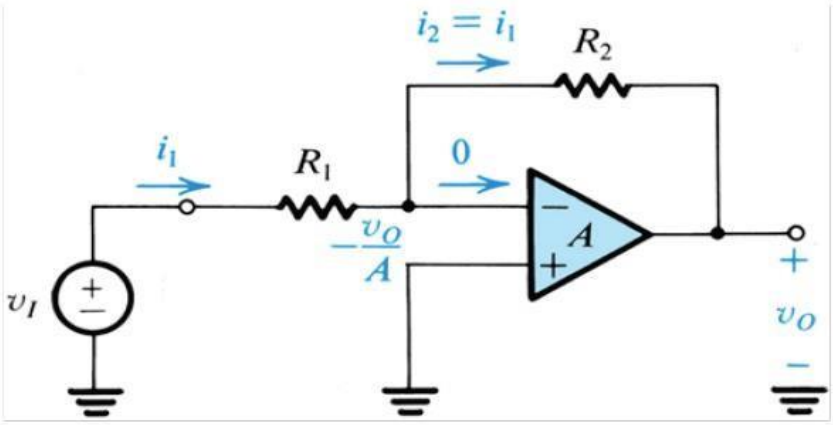
ii. It also means that the closed-loop gain is (ideally) independent of the opamp gain.

Effect of Finite Open-Loop Gain

The points just made are more clearly illustrated by deriving an expression for the closedloop gain under the assumption that the op-amp open-loop gain A is finite. Figure 5.7shows the analysis. If we denote the output voltage v_0 , then the voltage between the two input v^0/A . Since the positive input terminal is grounded, the terminals of the op amp will be

v^0/A. voltage

at the negative input terminal must be−



.

The current i_1 through R_1 can now be found from,

$$i_1 = \frac{v_I - (-v_0/A)}{R_1} = \frac{v_I + v_0/A}{R_1}$$

The infinite input impedance of the op amp forces the currenti_1 to flow entirely through R_2 . The output voltage v_0 can thus be determined from

$$v_0 = -\frac{v_0}{A} - i_1 R_2$$

$$v_0 = -\frac{v_0}{A} - (\frac{v_I + v_0/A}{R_1})R_2$$

The closed-loop gain G is

$$G = \frac{v_0}{v_I} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

Note

i. As **A** approaches ∞, ***G*** approaches the ideal value of $-R_2/R_1$.

ii. As **A** approaches ∞, the voltage at the inverting input terminal approaches zero. This is the virtual-ground assumption we used in our earlier analysis when the op amp was assumed to be ideal.

iii. to minimize the dependence of the closed loop gain ***G*** on the value of the open-loop gain **A,** we should make

$$1 + R^2/R_1 \ll 1$$

An Important Application-The Inverting Weighted Summer

A very important application of the inverting configuration is the weighted-summer circuit shown in Fig. Here we have a resistance R_f in the negative-feedback path (as before), but we have a number of input signals $v_1, v_2 \ldots \ldots, v_n$ applied to a corresponding resistor $R_1, R_2 \ldots \ldots, R_n$ which are connected to the inverting terminal of the op amp. The ideal op amp will have a virtual ground appearing at its negative input terminal. Ohm's law then tells us that the currents $i_1, i_2 \ldots \ldots, i_n$ are given by

$$i_1 = \frac{v_1}{R_1}, \quad i_2 = \frac{v_2}{R_2}, \quad \ldots \ldots, i_n = \frac{v_n}{R_n}$$

All these currents sum together to produce the current i; that is,

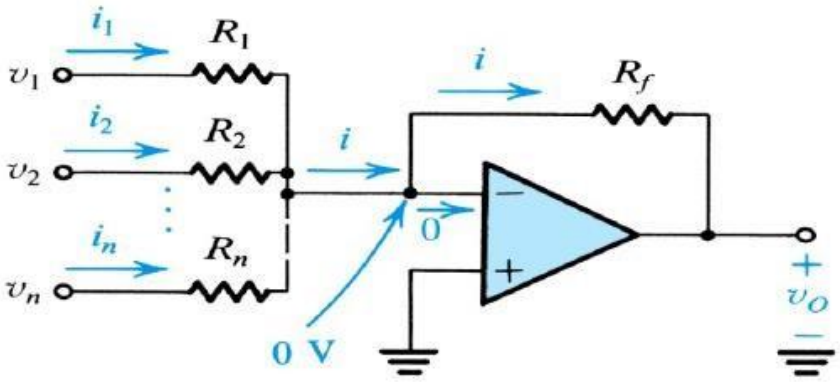
$$i = i_1 + i_2 + \cdots \ldots . . + i_n$$

will be forced to flow through R_f (since no current flows into the input terminals of an ideal op amp). The output voltage $v_0$may now be determined by another application of Ohm's law,

$$v_0 = 0 - iR_f = -iR_f$$

Thus,

$$v_0 = -(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \cdots \ldots . + \frac{R_f}{R_n} v_n)$$

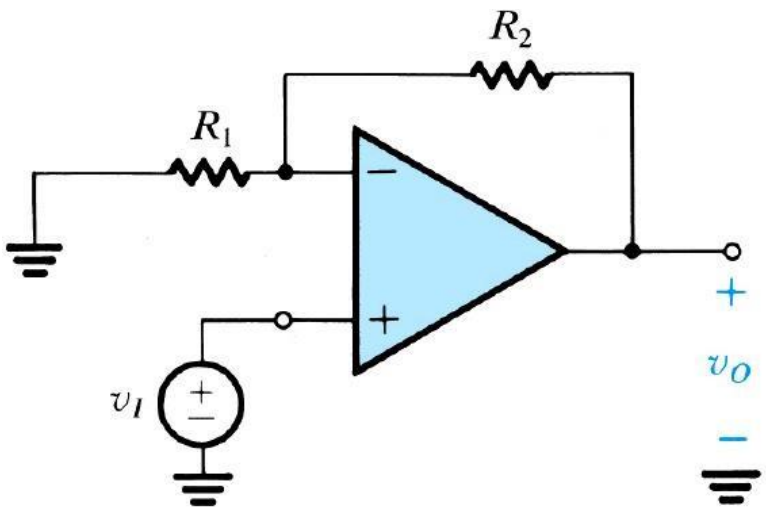


$$v_O = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \cdots + \frac{R_f}{R_n} v_n\right)$$

That is, the output voltage is a weighted sum of the input signalsv_1, v_2 … … , v_n. This circuit is therefore called a **weighted summer.**

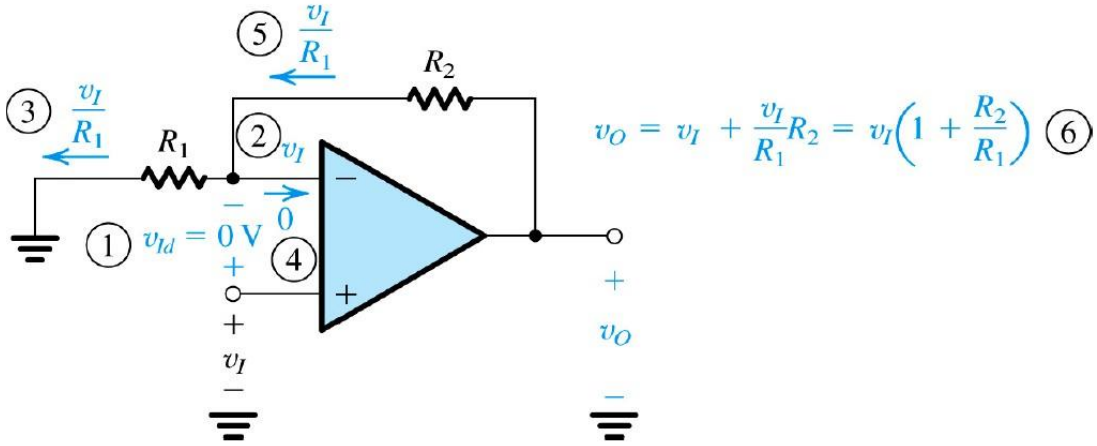
The Non inverting Configuration

The second closed-loop configuration we shall study is shown in Fig. Here the input signal $v_I$is applied directly to the positive input terminal of the op amp while one terminal of $R_1$is connected to ground.



The Closed-Loop Gain

Analysis of the non-inverting circuit to determine its closed-loop gain (v^0/v_i) is illustrated in Fig. Notice that the order of the steps in the analysis is indicated by circled numbers.



Assuming that the op amp is ideal with infinite gain, a virtual short circuit exists between its two input terminals. Hence the difference input signal is

$$v_{Id} = \frac{v_0}{A} = 0 \qquad for\ A = \infty$$

Thus the voltage at the inverting input terminal will be equal to that at the non-inverting input terminal, which is the applied voltage v_I . The current through R_1 can then be

v^I/R_1. Because of the infinite input impedance of the op amp, this current will determined as
flow through R_2as shown in Fig. Now the output voltage can be determined

from

$$v_0 = v_I + (\frac{v_I}{R_1})R_2$$

$$\boxed{\frac{v_0}{v_I} = 1 + \frac{R_2}{R_1}}$$

Note

If $v_I$increases, v_{Id} increases causing v_0 to increase as a result of the high (ideally infinite) gain of the op amp. However, a fraction of the increase in v_0 will be fed back to the inverting input terminal of the op amp through the (R_2, R_1) voltage divider. The result of this feedback will be to counteract the increase in, v_{Id}driving v_{Id} back to zero. This *degenerative* action of negative

feedback gives it the alternative name **degenerative feedback.** Finally, note that the argument above applies equally well if v_I decreases.

Effect of Finite Open-Loop Gain

Let us consider the effect of the finite op-amp open-loop gain A on the gain of the non inverting configuration. Assuming the op amp to be ideal, except for having a finite open loop gain A, it can be shown that the closed-loop gain of the non-inverting amplifier circuit of Fig. is given by

$$A \qquad G = \frac{v_0}{v_I} = \frac{1 + (R_2/R_1)}{1 + \frac{R}{A}}$$

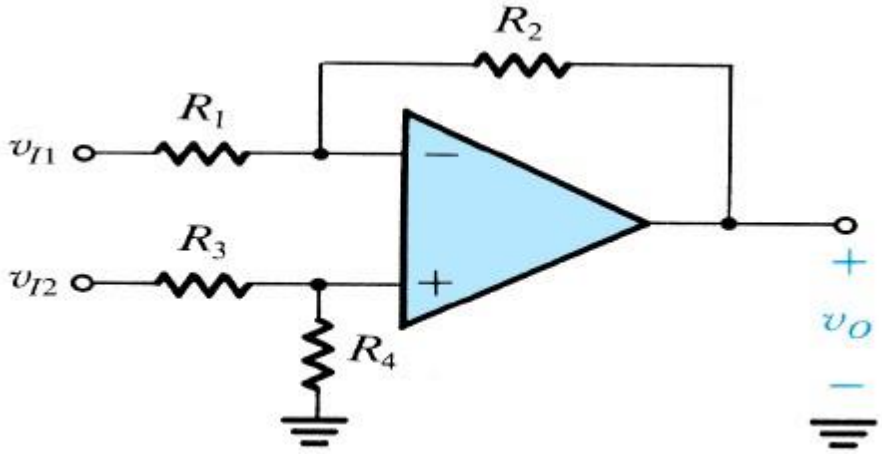
Observe that the denominator is identical to that for the case of the inverting configuration, because it is a result of the fact that both the inverting and the non-inverting configurations have the same feedback loop, which can be readily seen if the input signal source is eliminated (i.e., short-circuited). The numerators, however, are different, for the numerator $1 + R_2/R_1$ for the inverting configuration, and $-$ gives the ideal or nominal closed-loop gain, R_2/R_1 for the non inverting configuration. The gain expression in Eq. reduces to the ideal value of for

$$A = \frac{R_2}{R_1} \gg 1$$

DIFFERENCE AMPLIFIERS

It is one of the very important applications of Op amp. A difference amplifier is one that responds to the **difference between** the **two signals applied at its input** and ideally rejects signals that are common to the two inputs. Design of a difference amplifier is motivated by the observation that the gain of the non inverting amplifier configuration is positive, $(1 + R_2/R_1)$, while that of the inverting configuration is negative, $(- R_2/R_1)$. Combining the two configurations together is then a step in the right direction—namely, getting the difference

between two input signals. The two gain magnitudes should be made equal in order to reject common-mode signals.



This, however, can be easily achieved by attenuating the positive input signal to reduce the gain of the positive path from,$(1 + R^2/R_1)$, to (R_2/R_1). The resulting circuit would then look like that shown in Fig. 5.16, where the attenuation in the positive input path is achieved by the voltage divider $(R_3 - R_4)$**.** The proper ratio of this voltage divider can be determined from

$$\frac{R_4}{R_3 + R_4}\left(1 + \frac{R_2}{R_1}\right) = \frac{R_2}{R_1}$$

This can be put in the form

$$\frac{R_4}{R_3 + R_4} = \frac{R_2}{R_1 + R_2}$$

This condition satisfied by selecting

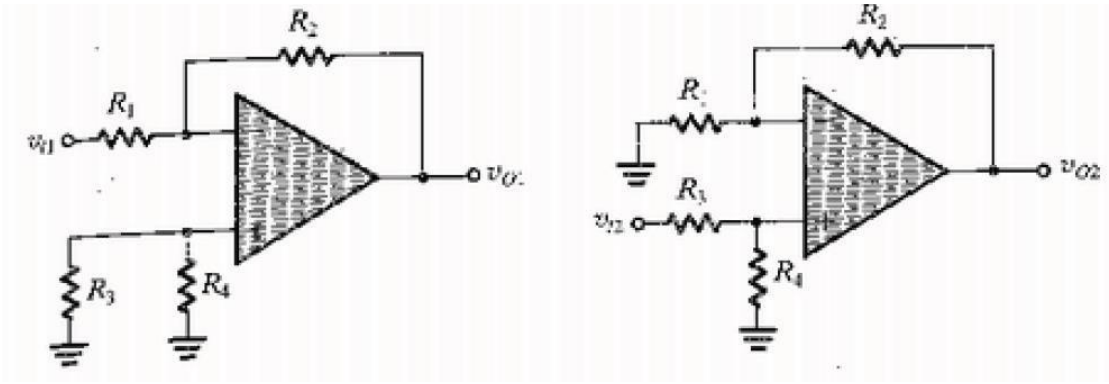
$$\frac{R_2}{R_1} = \frac{R_3}{R_4}$$

Since, the circuit is linear, we can use superposition.

To apply superposition, we first reduce v_{I2} to zero—that is, ground the terminal to which v_{I2} is applied and then find the corresponding output voltage, which will be due entirely to v_{I2}.We denote this output voltage v_{01} and its value may be found from the circuit in Fig.(a), which we

recognize as that of the inverting configuration. The existence of R_3 and R_4 does not affect the gain expression, since no current flows through either of them. Thus,

$$v_{01} = -\frac{R_2}{R_1} v_{i1}$$



Next, we reduce v_{I1} to zero and evaluate the corresponding output voltagev_{02}. The circuit will now take the form shown in Fig.(b), which we recognize as the non inverting configuration with an additional voltage divider, made up of R_3 and R_4 and connected to the input v_{I2}The output voltage v_{02} is therefore given by

$$\boldsymbol{v_{02}} = \boldsymbol{v_{I2}} \frac{R_4}{R_3 + R_4}\left(1 + \frac{R_2}{R_1}\right) = \frac{R_2}{R_1} v_{i2}$$

The superposition principle tells us that the output voltage v_0 is equal to the sum of $v_{01}and$ v_{02}Thus we have

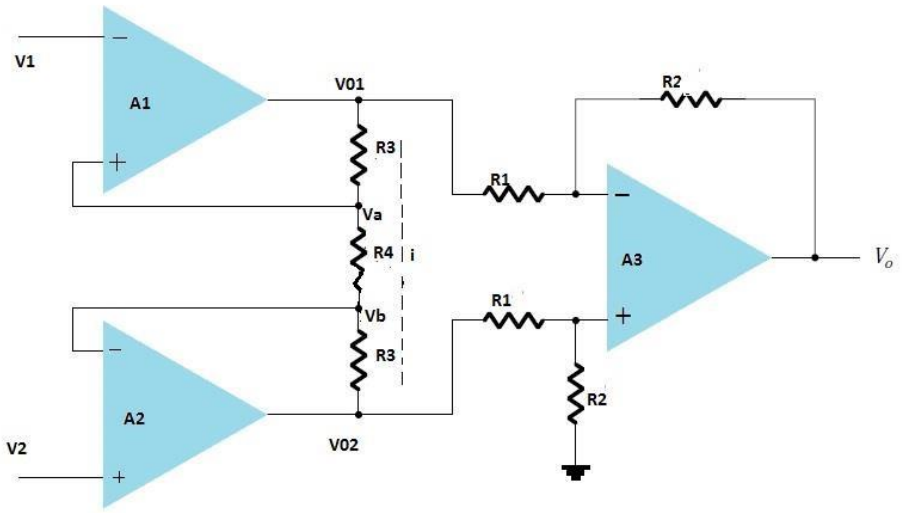
$$v0 = v01 + v02$$

$$\boxed{v_0 = \frac{R_2}{R_1}(v_{i2} - v_{i1})}$$

A Superior Circuit-The Instrumentation Amplifier

The low-input-resistance problem of the difference amplifier of can be solved by buffering the two input terminals using voltage followers; that is, a voltage follower is connected between each input terminal and the corresponding input terminal of the difference amplifier. Also additional voltage gain can also be obtained. It is especially interesting, that we can achieve this without compromising the high input resistance simply by using followers-with-gain rather than unity-gain followers. Bulk of the Gain is achieved in this new first stage i.e. the differential amplifier, which eases the burden on the difference amplifier in the second stage, leaving it to its main task of implementing the differencing function and thus rejecting common-mode signals.

The resulting circuit is shown in Fig. It consists of two stages. The first stage is formed by op amps A_1 and A_2 , and their associated resistors, and the second stage is the difference amplifier formed by op amp A_3 and its four associated resistors. Observe that, each of and is connected in the non inverting configuration.



The output of amplifier A_1 and A_2 are labelled as V_{01} and V_{02} respectively. Since the amplifier A_3 is a difference one, the output voltage is given by,

$$V_0 = \frac{R_2}{R_1}(V_{02} - V_{01})$$

From amplifier A_1

$$V_1 = V_a$$

From amplifier A_2

$$V_2 = V_b$$

The current

$$i = \frac{V_a - V_b}{R_4} = \frac{V_1 - V_2}{R_4}$$

The differences between output voltages of amplifiers A_1 and A_2 is

$$V_{02} - V_{01} = i(2R_3 + R_4)$$

Now, the output voltage is,

$$V_0 = \frac{R_2}{R_1}(V_{02} - V_{01})$$

$$\boxed{V_0 = \frac{R_2}{R_1}\left(\frac{V_1 - V_2}{R_4}\right)(2R_3 + R_4)}$$

Advantages:

i. Very high (ideally infinite) input resistance ii. High differential gain iii. High CMRR iv. Low Output Resistance

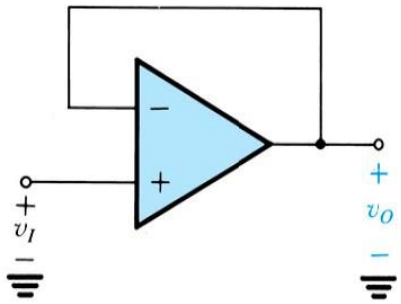
Slew Rate

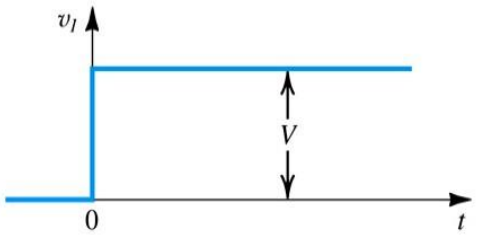
Another phenomenon that can cause nonlinear distortion when large output signals are present is that of slew-rate limiting. This refers to the fact that there is a specific maximum rate of change possible at the output of a real op amp. This maximum is known as the slew rate (SR) of the op amp and is defined as

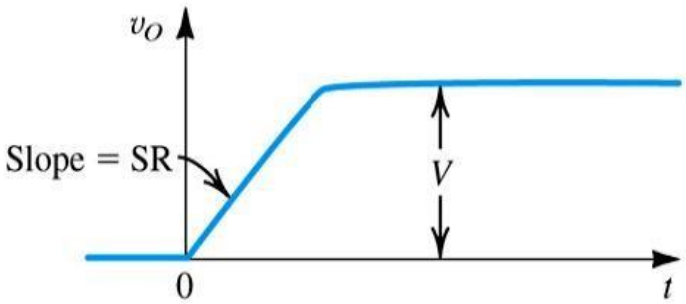
$$SR = \frac{dv_0}{dt}|max$$

and is usually specified on the op-amp data sheet in units of V/µs. It follows that if the input signal applied to an op-amp circuit is such that it demands an output response that is faster than the specified value of SR, the op amp will not comply. Rather, its output will change at the maximum possible rate, which is equal to its SR.

As an example, consider an op amp connected in the unity-gain voltage-follower configuration shown in Fig.(a), and let the input signal be the step voltage shown in Fig.(b). The output of the op amp will not be able to rise instantaneously to the ideal value V; rather, the output will be the linear ramp of slope equal to SR, shown in Fig.(c). The amplifier is then said to be slewing, and its output is slew-rate limited.





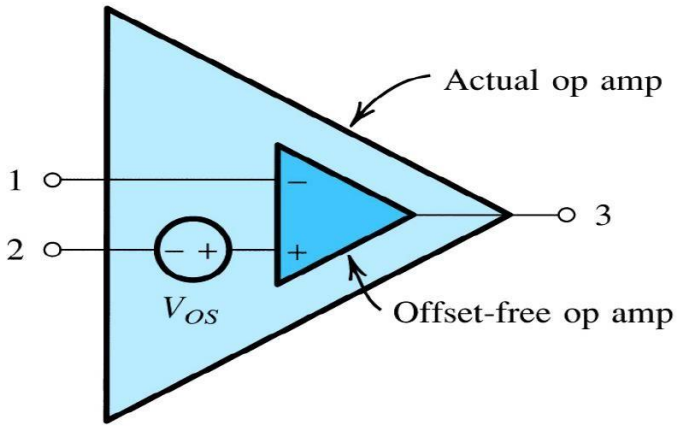


OP-AMP SPECIFICATIONS—DC

OFFSET PARAMETERS

Offset Voltage

Because op amps are direct-coupled devices with large gains at dc, they are prone to dc problems. The first such problem is the dc offset voltage. To understand this problem consider the following *conceptual* experiment; If the two input terminals of the op amp are tied together and connected to ground, it will be found that a finite dc voltage exists at the output. In fact, if the op amp has a high dc gain, the output will be at either the positive or negative saturation level. The op-amp output can be brought back to its ideal value of 0 V by connecting a dc voltage source of appropriate polarity and magnitude between the two input terminals of the op amp. This external source balances out the input offset voltage of the op amp. It follows that the input offset voltageV_{os} must be of equal magnitude and of opposite polarity to the voltage we applied externally.



The input offset voltage arises as a result of the unavoidable mismatches present in the input differential stage inside the op amp. The effect of on the operation of closed-loop opamp circuits are:

i. General-purpose op amps exhibit V_{os} in the range of 1 mV to 5 mV.

ii. Also, the value of V_{os} depends on temperature. The op-amp data sheets usually specify typical and maximum values for V_{os} at room temperature as well as the temperature coefficient of V_{os} (usually in μV/°C). They do not, however, specify the polarity of V_{os} because the component mismatches that give rise to V_{os} are obviously not known apriori.

iii. Different units of the same op-amp type may exhibit either a positive or a negativeV_{os}.

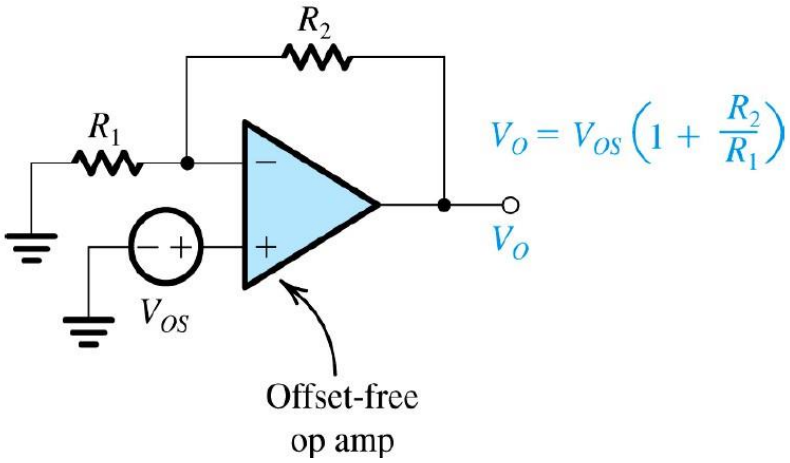
To analyze the effect of on operation of op-amp circuits, we need a circuit model for the op amp with input offset voltage. Such a model is shown in Fig. It consists of a dc source of value

placed in series with the positive input lead of an offset-free op amp. The justification for this model follows from the description above.

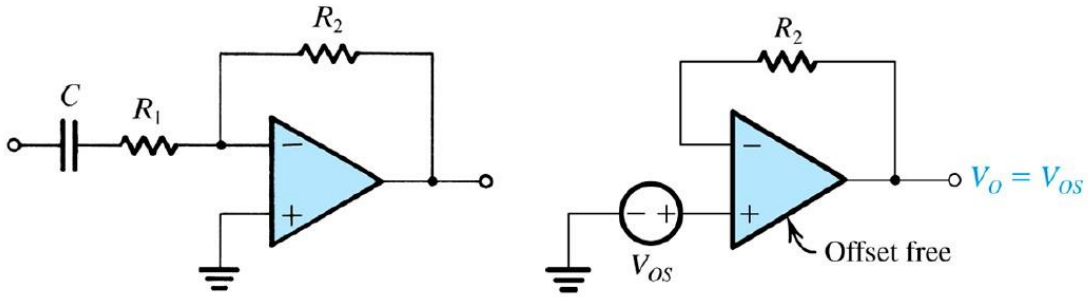
Analysis:

The input voltage signal source is short circuited and the op amp is replaced with the model of Fig. (Eliminating the input signal, done to simplify, is based on the principle of superposition.) Following this procedure we find that both the inverting and the non inverting amplifier configurations result in the same circuit, that shown in Fig., from which the output dc voltage due to V_{os} is found to be

$$V_0 = V_{os}(1 + \frac{R_2}{R_1})$$



One way to overcome the dc offset problem is by capacitively coupling the amplifier. This will be possible only in applications where the closed-loop amplifier is not required to amplify dc or very low frequency signals. Figure shows a capacitively coupled amplifier. Because of its infinite impedance at dc, the coupling capacitor will cause the gain to be zero at dc. As a result the equivalent circuit for determining the dc output voltage resulting from the op-amp input offset voltage will be that shown in Fig.



Input Bias and Offset Currents

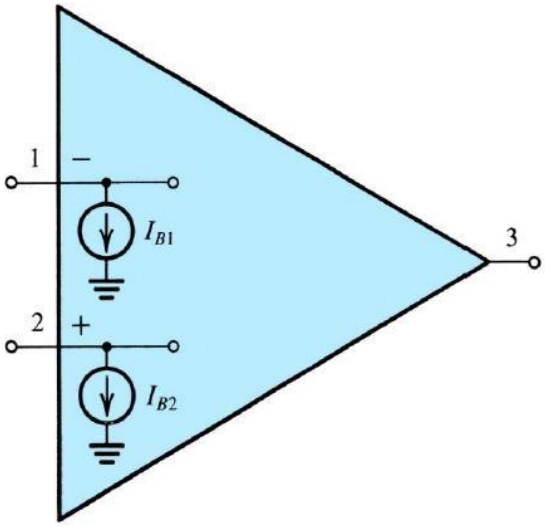
The second dc problem encountered in op amps is illustrated in Fig. In order for the op amp to operate, its two input terminals have to be supplied with dc currents, termed the **input bias currents.** In Fig. these two currents are represented by two current sources,I_{B1} andI_{B2}, connected to the two input terminals. It should be emphasized that the input bias currents are independent of the fact that a real op amp has finite though large input resistance. The op-amp manufacturer usually specifies the average value of $I_{B1}$and I_{B2}as well as their expected difference. The average valueI_B is called the **input bias current,**

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

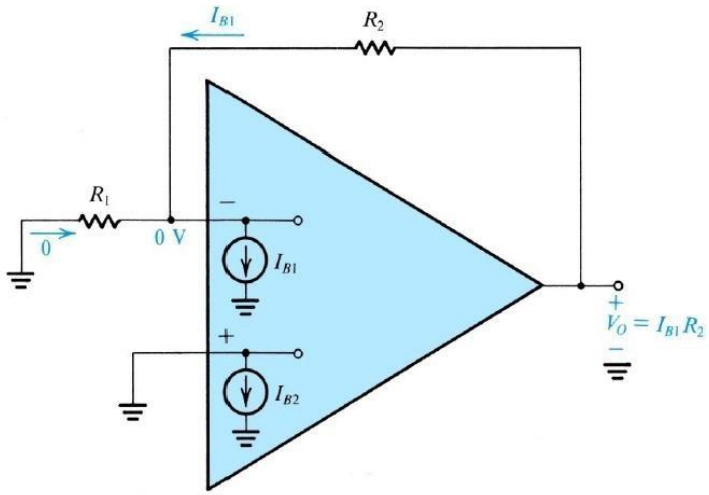
and the difference is called the **input offset current** and is given by

$$I_{OS} = |I_{B1} - I_{B2}|$$

Typical values for general-purpose op amps that use bipolar transistors are$I_B = 100nA$ and $I_{OS} = 10nA$. Op amps that utilize field-effect transistors in the input stage have a much smaller input bias current (of the order of pico amperes).



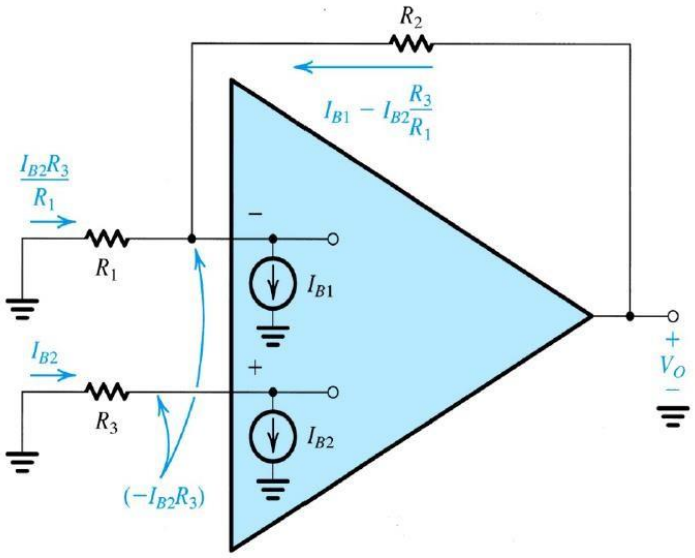
To find the dc output voltage of the closed-loop amplifier due to the input bias currents, we ground the signal source and obtain the circuit shown in Fig. 5.40 for both the inverting and non inverting configurations.



As shown in Fig., the output dc voltage is given by,

$$V_0 = I_{B1}R_2 = I_BR_2$$

This obviously places an upper limit on the value of R_2 .Fortunately; however, a technique exists for reducing the value of the output dc voltage due to the input bias currents. The method consists of introducing a resistance R_3 in series with the non inverting input lead, as shown in Fig. From a signal point of view,R_3, has a negligible effect (ideally no effect).

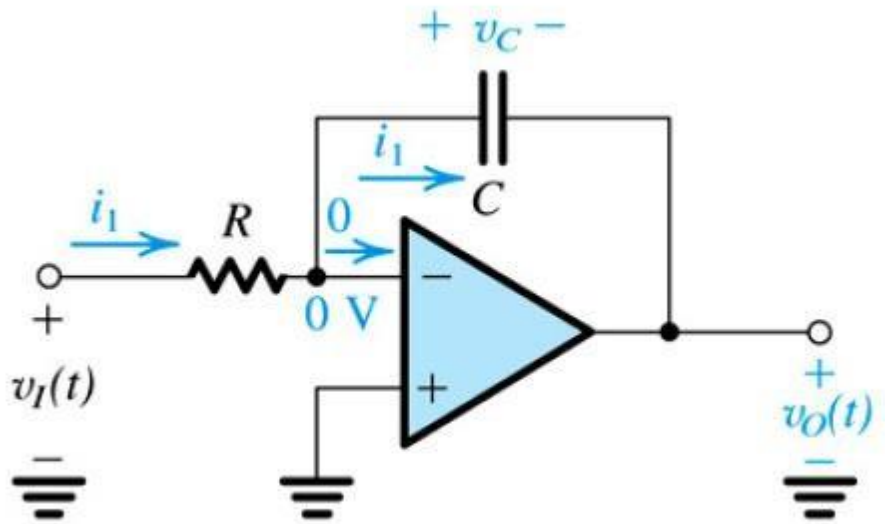


Integrators and Differentiators

The op-amp circuit applications discussed so far, utilized resistors in the op-amp feedback path and in connecting the signal source to the circuit, that is, in the feed-in path. As a result circuit operation has been (ideally) independent of frequency. The only exception has been the use of coupling capacitors in order to minimize the effect of the dc imperfections of op amps. By allowing the use of capacitors together with resistors in the feedback and feed-in paths of op-amp circuits, a very wide range of useful and exciting applications of the op amp can be obtained. We begin our study of op-amp-RC circuits in this section by considering two basic applications, namely signal integrators and differentiators.

The Inverting Integrator

By placing a capacitor in the feedback path and a resistor at the input, we shall now show that this circuit realizes the mathematical operation of integration. Let the input be a time varying function$v_I(t)$. The virtual ground at the inverting op-amp input causes $v_I(t)$ to appear in effect across *R,* and thus the current will be $v_I(t)/R$. This current flows through the capacitor C, causing charge to accumulate on C.



The current through the resistor R

$$i_1 = v^I(t) - 0/R = v_I(t)/R$$

The current through the capacitor C

$$i_C = C\frac{dV}{dt}$$

$$= C\frac{d(0 - v_0)}{dt}$$

$$i_C = -C\frac{dv_0}{dt}$$

Both currents are equal because ideal op amp draws no current to its input terminals. So,

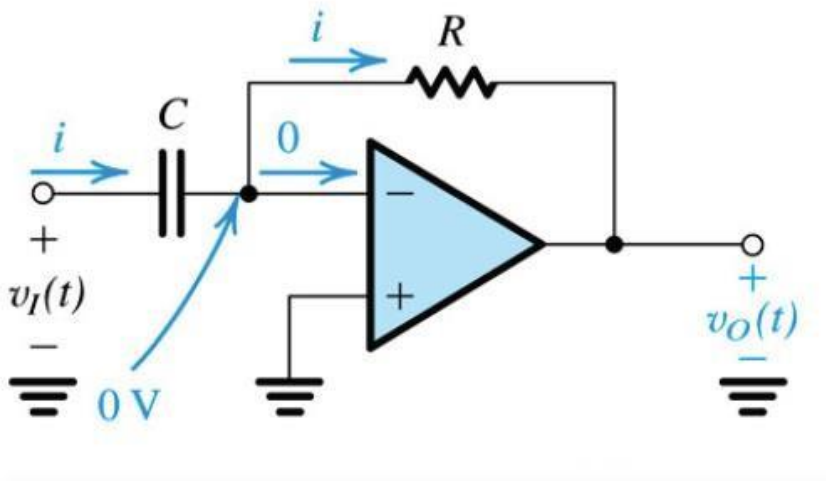
$$v_I(t)/_R = -C\frac{dv_0}{dt}$$

$$\int dv_0 = -\frac{1}{RC}\int v_I(t)dt$$

$$\boxed{v_0 = -\frac{1}{RC}\int v_I(t)dt}$$

The Op-Amp Differentiator

Interchanging the location of the capacitor and the resistor of the integrator circuit results in the circuit in Fig., which performs the mathematical function of differentiation. To see how this comes about, let the input be the time-varying function $v_I(t)$ and note that the virtual ground at the inverting input terminal of the op amp causes $v_I(t)$ to appear in effect across the capacitor *C.* Thus the current through C will be $C\frac{dv_I}{dt}$ and this current flows through the feedback resistor R providing at the op-amp output a voltage $v_0(t)$.



The current through the capacitor C

$$i_C = C\frac{d(v_I - 0)}{dt}$$

$$= C\frac{dv_I(t)}{dt}$$

The current through the resistor R

$$i_R = \frac{0 - v_0}{R} = -\frac{v_0}{R}$$

Both currents are equal because ideal op amp draws no current to its input terminals. So,

$$-\frac{v_0}{R} = C\frac{dv_I(t)}{dt}$$

$$\boxed{v_0 = -RC\frac{dv_I(t)}{dt}}$$

Power Amplifier

Prepared by:

DEBASISH MOHANTA

Assistant Professor

Department of Electrical Engineering

GCE, Keonjhar

Reference: **"Electronic Devices and Circuit Theory"**

Robert L. Boylestad and L. Nashelsky

Power Amplifiers

Introduction

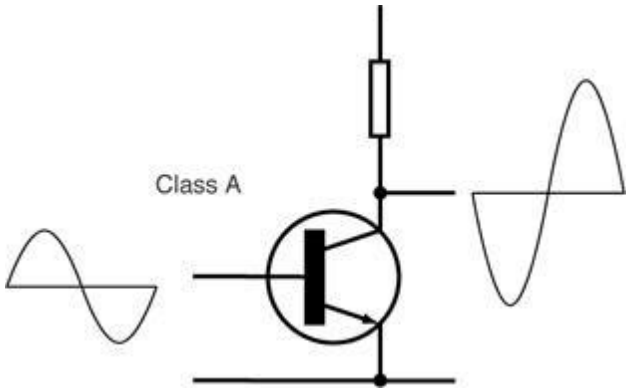
- ✓ Amplifier receives a signal from some pickup transducer or other input source and provides larger version of the signal.
- ✓ In small signal amplifiers the main factors are usually amplification, linearity and magnitude of gain.

Classes of Power Amplifiers

- ✓ Amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal.
- ✓ So the following classes of PA are defined:
  - Class A
  - Class B
  - Class AB
  - Class C
  - Class D

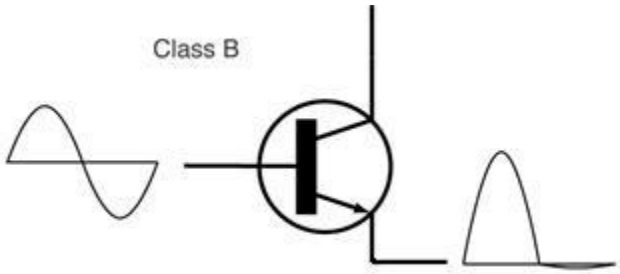
Class A amplifier

- ✓ Class A amplifying devices operate over the whole of the input cycle such that the output signal is an exact scaled-up replica of the input with no clipping.
- ✓ Class A amplifiers are the usual means of implementing small signal amplifiers.
- ✓ They are not very efficient; a theoretical maximum of 50% is obtainable with inductive output coupling and only 25% with capacitive coupling.
- ✓ In a Class A circuit, the amplifying element is biased so the device is always conducting to some extent, and is operated over the most linear portion of its characteristic curve.
- ✓ Because the device is always conducting, even if there is no input at all, power is drawn from the power supply. This is the chief reason for its inefficiency.



Class B amplifier

- ✓ Class B amplifiers only amplify half of the input wave cycle.
- ✓ As such they create a large amount of distortion, but their efficiency is greatly improved and is much better than Class A.
- ✓ Class B has a maximum theoretical efficiency of 78.5% (i.e., $\pi/4$). This is because the amplifying element is switched off altogether half of the time, and so cannot dissipate power.
- ✓ A single Class B element is rarely found in practice, though it can be used in RF power amplifier where the distortion levels are less important. However Class C is more commonly used for this.

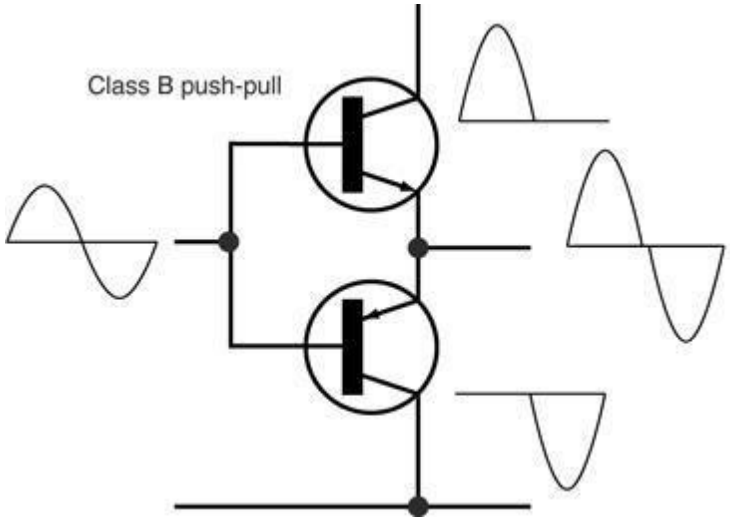


Class AB amplifier

- ✓ A practical circuit using Class B elements is the complementary pair or "pushpull" arrangement.
- ✓ Here, complementary or quasi-complementary devices are used to each amplify the opposite halves of the input signal, which is then recombined at the output.

- ✓ This arrangement gives excellent efficiency, but can suffer from the drawback that there is a small mismatch at the "joins" between the two halves of the signal.

- ✓ Class AB sacrifices some efficiency over class B in favour of linearity, so will always be less efficient (below 78.5%). It is typically much more efficient than class A.

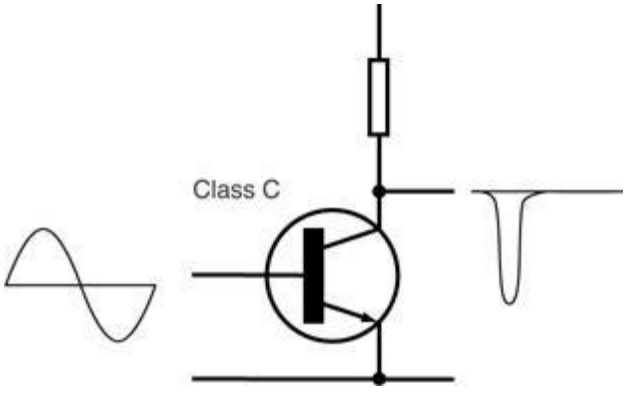


Class C amplifier

- ✓ Class C amplifiers conduct less than 50% of the input signal and the distortion at the output is high, but high efficiencies (up to 90%) are possible.

- ✓ A much more common application for Class C amplifiers is in RF transmitters, where the distortion can be vastly reduced by using tuned loads on the amplifier stage.

- ✓ The input signal is used to roughly switch the amplifying device on and off, which causes pulses of current to flow through a tuned circuit.



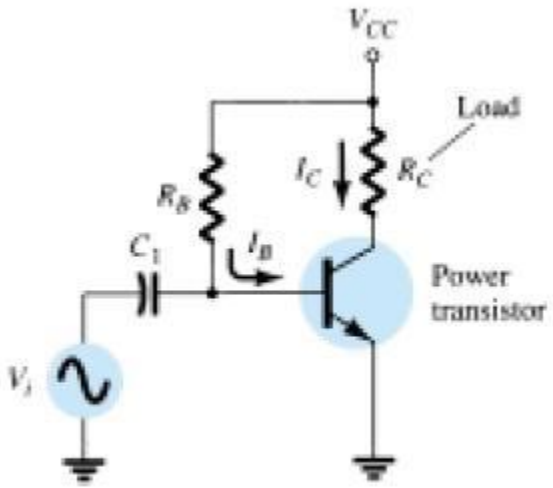
Class D amplifier

- ✓ Class D amplifiers are much more efficient than Class AB power amplifiers.
- ✓ As such, Class D amplifiers do not need large transformers and heavy heat sinks, which means that they are smaller and lighter in weight than an equivalent Class AB amplifier.
- ✓ All power devices in a Class D amplifier are operated in on/off mode.
- ✓ These amplifiers use pulse width modulation.

Comparison of Amplifier classes

Parameters	A	AB	B	C	D
Operating Cycle	360_0	180^0-360^0	180^0	Less than 180^0	Pulse operation
Power efficiency	25-50%	Between 25%(50%) and 78.5%	78.5%		Typically over 90%

Series fed class A amplifiers



- ✓ It is a fixed bias circuit.

- ✓ The transistor used is a power transistor that is capable of operating in the range of a few to tens of watts.
- ✓ This circuit is not the best to use as a large-signal amplifier because of its poor power efficiency.

- ✓ The beta of a power transistor is generally less than 100, the overall amplifier circuit using power transistors that are capable of handling large power or current while not providing much voltage gain.

DC bias operation

- ✓ The dc bias set by $V_{CC}$and $R_B$fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7\text{V}}{R_B}$$

with the collector current then being

$$I_C = \beta I_B$$

with the collector–emitter voltage then

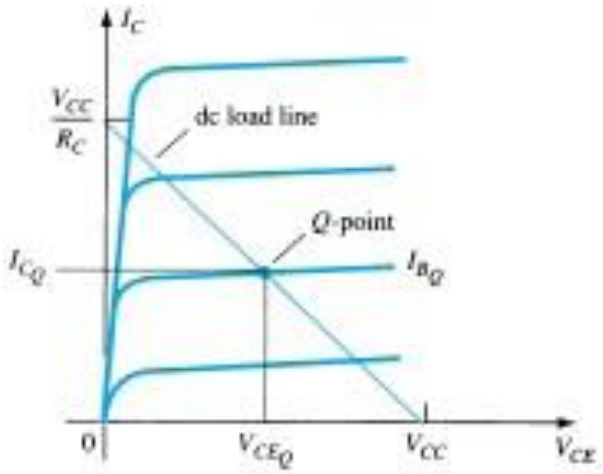
$$V_{CE} = V_{CC} - I_C R_C$$

- ✓ To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig.

- ✓ The intersection of the dc bias value of I_B with the dc load line then determines the operating point (Q-point) for the circuit.

- ✓ If the dc bias collector current is set at one-half the possible signal swing (between 0 and V_{CC}/R_C), the largest collector current swing will be possible.

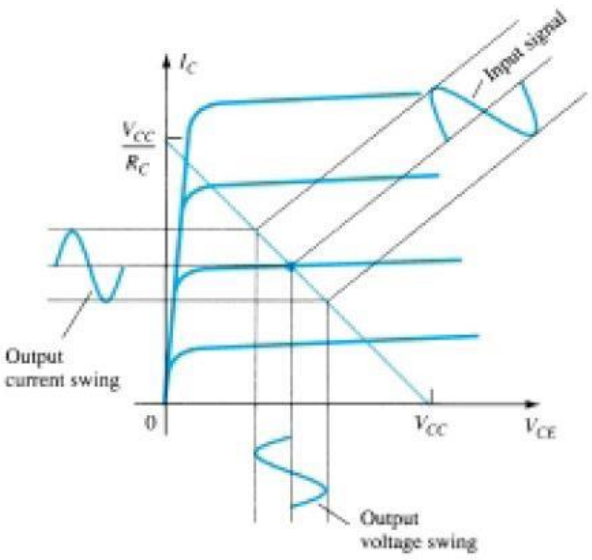
- ✓ Additionally, if the quiescent collector-emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible.



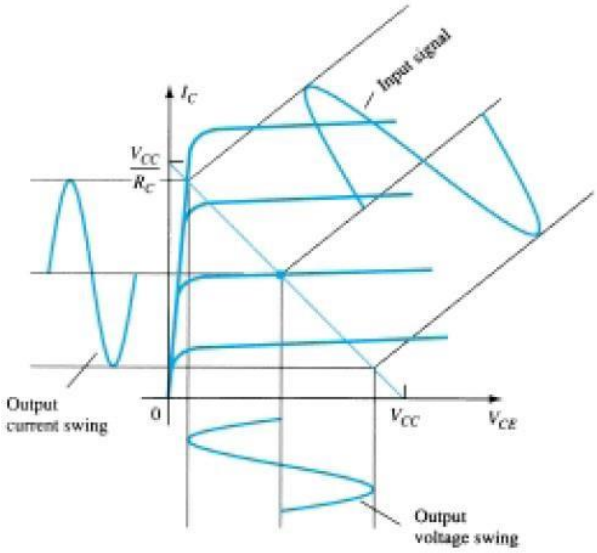
AC Operation

- ✓ When an input ac signal is applied to the amplifier, the output will vary from its dc bias operating voltage and current.

- ✓ A small input signal, as shown in Fig., will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well as the collector–emitter voltage to vary around its dc bias value.



- ✓ As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition.



- ✓ For the current this limiting condition is either zero current at the low end or V_{CC}/R_C at the high end of its swing.
- ✓ For the collector–emitter voltage, the limit is either 0 V or the supply voltage V_{CC}.

Power Considerations

- ✓ The power into an amplifier is provided by the supply.

- ✓ With no input signal, the dc current drawn is the collector bias current, I_{CQ}.

- ✓ The power then drawn from the supply is

$$P_i(dc) = V_{CC}I_{CQ}$$

Output power

- ✓ The output voltage and current varying around the bias point provide ac power to the load.

- ✓ The ac signal, V_i, causes the base current to vary around the dc bias current and the collector current around its quiescent level, I_{CQ}.

- ✓ The larger the input signal, the larger the output swing, up to the maximum set by the circuit.

Using rms signals

$$P_0(ac) = V_{CE}(rms)I_C(rms)$$

$$= I_C^2(rms)R_C$$

$$= \frac{V_C^2(rms)}{R_C}$$

Using peak signals

The ac power delivered to the load may be expressed using

$$P_0(ac) = \frac{V_{CE}(p)I_C(p)}{2}$$

$$= \frac{I_C^2(p)}{2}R_C$$

$$= \frac{V_{CE}{}^2(p)}{2R_C}$$

Using peak-to-peak signals

The ac power delivered to the load may be expressed using

$$P_0(ac) = \frac{V_{CE}(pp)I_C(pp)}{8}$$

$$= \frac{I_C{}^2(pp)}{8}R_C$$

$$= \frac{V_{CE}{}^2(pp)}{8R_C}$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\%\eta = \frac{P_0(ac)}{P_i(dc)} \times 100\%$$

Maximum Efficiency

- ✓ For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings.
- ✓ For the voltage swing it is

$$V_{CE}(pp) = V_{CC}$$

- ✓ For the current swing it is

$$I_C(pp) = \frac{V_{CC}}{R_C}$$

- ✓ Using the maximum voltage swing in the equation below yields

$$P_0(ac) = \frac{V_{CE}(pp)I_C(pp)}{8}$$

$$= \frac{V_{CC}\, {}^{V_{CC}}/_{R_C}}{8}$$

$$= \frac{{V_{CC}}^2}{8R_C}$$

- ✓ The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

$$\text{Maximum } P_i(dc) = V_{CC}(\text{maximum} I_C) = V_{CC}\frac{V_{CC}/R_C}{2}$$

$$= \frac{{V_{CC}}^2}{2R_C}$$

- ✓ Then the maximum efficiency is given by,

$$\%\eta = \frac{P_0(ac)}{P_i(dc)} \times 100\%$$

$$= \frac{{V_{CC}}^2 / 8R_C}{{V_{CC}}^2 / 2R_C}$$

$$= 25\%$$

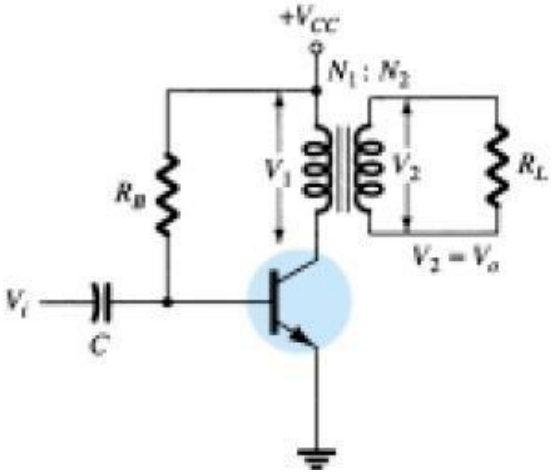
- ✓ The maximum efficiency of a class A series fed amplifier is thus seen to be 25%.

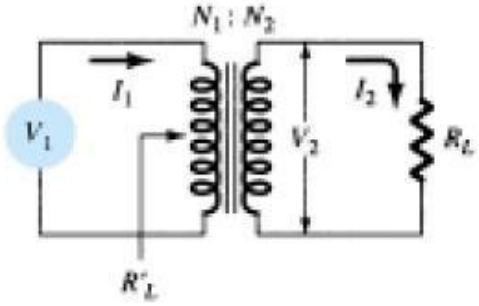
- ✓ The maximum efficiency occurs only for ideal conditions of both voltage and current swing .thus practical circuits will have less than this percentage.

TRANSFORMER-COUPLED CLASS A AMPLIFIER

- ✓ A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in Fig.

- ✓ The transformer can step up or step down a voltage applied to primary coil.



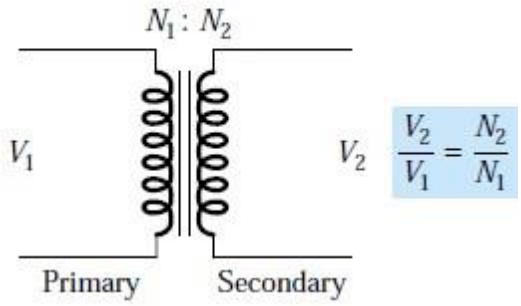


VOLTAGE TRANSFORMATION

- ✓ The transformer can step up or step down a voltage applied to one side directly as the ratio of the turns (or number of windings) on each side.

- ✓ The voltage transformation is given by

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$



$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

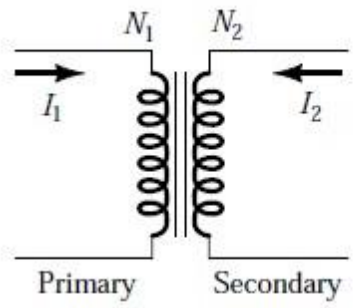
- ✓ Equation shows that if the number of turns of wire on the secondary side is larger than on the primary, the voltage at the secondary side is larger than the voltage at the primary side.

CURRENT TRANSFORMATION

- ✓ The current in the secondary winding is inversely proportional to the number of turns in the windings.

- ✓ The current transformation is given by

$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$



$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

- ✓ If the number of turns of wire on the secondary is greater than that on the primary, the secondary current will be less than the current in the primary.

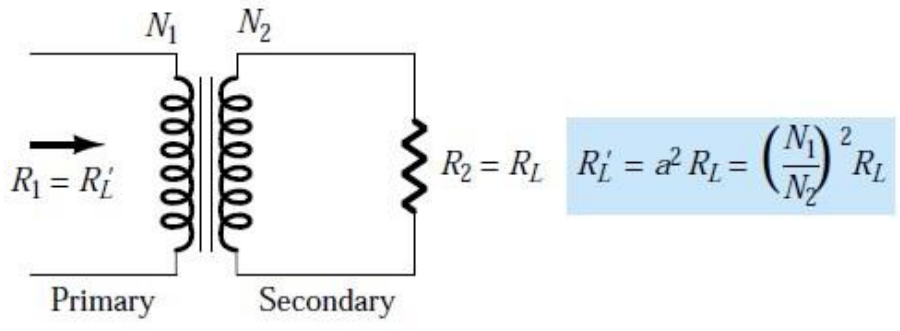
IMPEDANCE TRANSFORMATION

- ✓ Since the voltage and current can be changed by a transformer, an impedance "seen" from either side (primary or secondary) can also be changed.

- ✓ As shown in Fig, impedance R_L is connected across the transformer secondary.

- ✓ This impedance is changed by the transformer when viewed at the primary side ($R_L{}'$).

$$\frac{R_L}{R_L{}'} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2}{I_2}\frac{I_1}{V_1} = \frac{V_2}{V_1}\frac{I_1}{I_2} = \frac{N_2}{N_1}\frac{N_2}{N_1} = \left(\frac{N_2}{N_1}\right)^2$$



- ✓ If we define $a = \frac{N_1}{N_2}$, where a is the turns ratio of the transformer, the above equation becomes

$$\frac{R_L{}'}{R_L} = \frac{R_1}{R_2} = (\frac{N_1}{N_2})^2 = a^2$$

- ✓ We can express the load resistance reflected to the primary side as

$$\boxed{R_L{}' = a^2 R_L}$$

Where $R_L{}'$ is the reflected impedance.

Signal Swing and Output Ac Power

- ✓ Figure shows the voltage and current signal swings from the circuit of Transformer-coupled audio power amplifier.

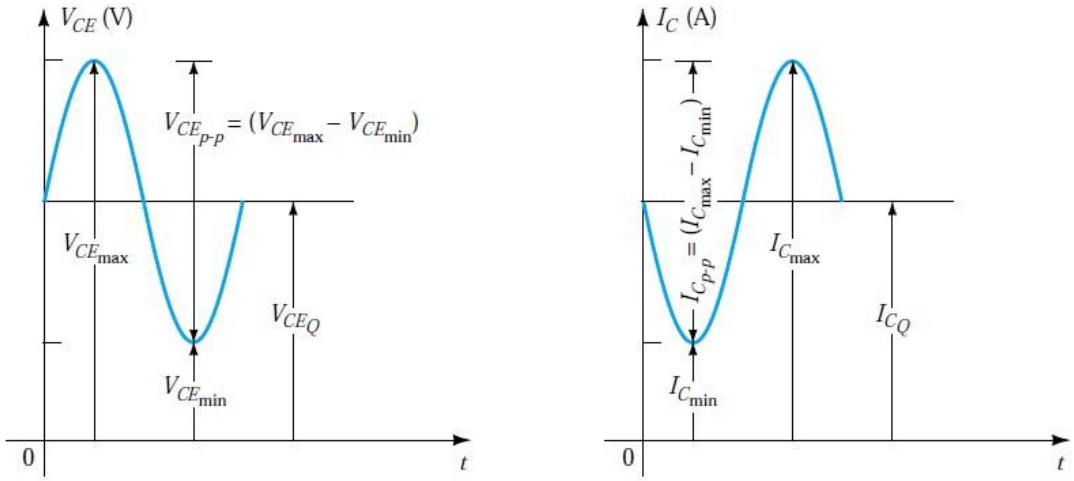
- ✓ From the signal variations shown in Fig, the values of the peak-to-peak Signal swings are

$$V_{CE}(pp) = V_{CEmax} - V_{CEmin}$$

$$I_C(pp) = I_{Cmax} - I_{Cmin}$$

- ✓ The ac power developed across the transformer primary can then be calculated using

$$P_0(ac) = \frac{(V_{CE_{max}} - V_{CE_{min}})(I_{C_{max}} - I_{C_{min}})}{8}$$



✓ For the ideal transformer, the voltage delivered to the load can be calculated using the following equation.

$$V_L = V_2 = \frac{N_2}{N_1} V_1$$

✓ The power across the load can then be expressed as

$$P_L = \frac{V_L{}^2(rms)}{R_L}$$

✓ Similarly the load current can be calculated as $I_L = I_2 = \frac{N_1}{N_2} I_C$ with the output ac power

$$P_L = I_L{}^2(rms)R_L$$

Efficiency

✓ The input dc power obtained from the supply is calculated from the supply dc voltage and thus average power drawn from the supply.

$$P_i(dc) = V_{CC}I_{CQ}$$

✓ For the transformer-coupled amplifier, the power dissipated by the transformer is small (due to the small dc resistance of a coil) and is ignored.

✓ The only power loss considered here is that dissipated by the power transistor and calculated by

$$P_Q = P_i(dc) - P_0(ac)$$

Where P_Q is the power dissipated as heat.

$$\%\eta = \frac{P_0(ac)}{P_i(dc)} \times 100\%$$

Maximum theoretical efficiency

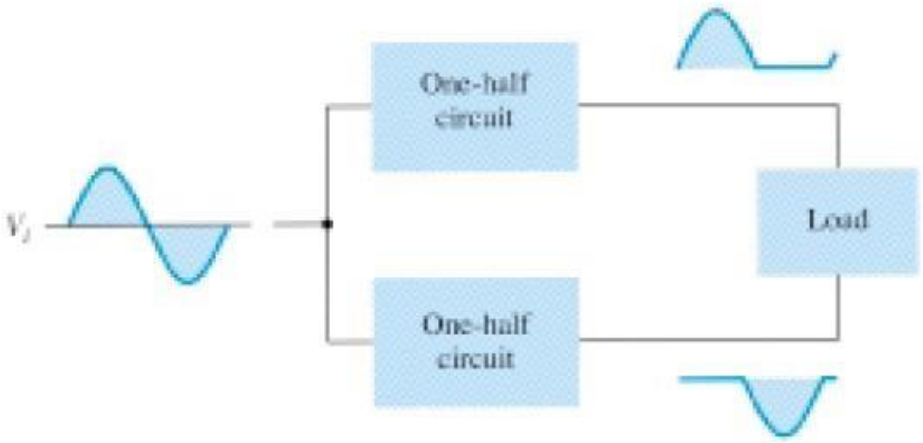
- ✓ For a class A transformer-coupled amplifier, the maximum theoretical efficiency goes up to 50%.
- ✓ Based on the signals obtained using the amplifier, the efficiency can be expressed as

$$\%\eta = 50\left(\frac{V_{CE_{max}} - V_{CE_{min}}}{V_{CE_{max}} + V_{CE_{min}}}\right)^2 \%$$

- ✓ Larger the value of V_{CEmax} and smaller the value of V_{CEmin}, the closer the efficiency approaches the theoretical limit of 50%.

Class B Amplifier operation

- ✓ Class B operation is provided when the dc bias leaves the transistor biased just off, the transistor turning on when the ac signal is applied.
- ✓ This is essentially no bias and conducts for only one half cycle.
- ✓ To obtain output for full cycle, it is required to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output on opposite half cycles of output signal.
- ✓ Since one part of the circuit pushes the signal high during one half cycle and other part pulls the signal low during the other half cycle, the circuit is referred to as push-pull circuit.
- ✓ Class B operation provides greater efficiency than was possible using single transistor in class A operation.



Input (DC) Power

✓ The amount of input power can be calculated using

$$P_i(dc) = V_{CC} I_{dc}$$

Where I_{dc} is the average or dc current drawn from the power supplies.

✓ In class B operation, the current drawn from a single power supply has the form of a full-wave rectified signal, while that drawn from two power supplies has the form of a half wave rectified signal from each supply.

✓ In either case, the value of the average current drawn can be expressed as

$$I_{dc} = \frac{2}{\pi} I(p)$$

where *I*(p) is the peak value of the output current waveform.

✓ Hence input power is equal to

$$\boxed{P_i(dc) = V_{CC} \frac{2}{\pi} I(p)}$$

Output (AC) Power

✓ The power delivered to the load (usually referred to as a resistance,R_L) can be calculated using any one of a number of equations.

✓ If one is using an rms meter to measure the voltage across the load, the output power can be calculated as

$$P_0(ac) = \frac{{V_L}^2(rms)}{R_L}$$

✓ If one is using an oscilloscope, the peak, or peak-to-peak, output voltage measured can be used:

$$P_0(ac) = \frac{V_L{}^2(pp)}{8R_L} = \frac{V_L{}^2(p)}{2R_L}$$

✓ The larger the rms or peak output voltage, the larger the power delivered to the load.

Efficiency

✓ The efficiency of the class B amplifier can be calculated using the basic equation:

$$\%\eta = \frac{P_0(ac)}{P_i(dc)} \times 100\%$$

$$= \frac{{V_L}^2(p)/2R_L}{V_{CC}\frac{2}{\pi}I(p)}$$

using $I(p) = V_L(p)/R_L$

$$\%\eta = \frac{\pi}{4}\frac{V_L(p)}{V_{CC}} \times 100\%$$

✓ Equation shows that the larger the peak voltage, the higher the circuit efficiency, up to a maximum value when $V_L(p) = V_{CC}$, this maximum efficiency then being

$$\text{maximum efficiency} = \frac{\pi}{4} \times 100\% = 78.5\%$$

Power dissipated by output transistors

✓ The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load.

$$P_{2Q} = P_i(dc) - P_0(ac)$$

where P_{2Q} is the power dissipated by the two output power transistors ✓

The dissipated power handled by each transistor is then

$$P_Q = \frac{P_{2Q}}{2}$$

Maximum Power Considerations

✓ For class B operation, the maximum output power is delivered to the load when $V_L(p) = V_{CC}$

$$maximum\ P_0(ac) = \frac{{V_{CC}}^2}{2R_L}$$

✓ The corresponding peak ac current I(p) is then

$$I(p) = \frac{V_{CC}}{R_L}$$

✓ The maximum value of average current from the power supply is

$$maximum\ I_{dc} = \frac{2}{\pi} I(p) = \frac{2}{\pi}\frac{V_{CC}}{R_L}$$

✓ Using this current to calculate the maximum value of input power results in

$$maximum\ P_i(dc) = V_{CC}(maximum\ I_{dc}) = V_{CC}\left(\frac{2}{\pi}\frac{V_{CC}}{R_L}\right) = \frac{2{V_{CC}}^2}{\pi R_L}$$

✓ The maximum circuit efficiency for class B operation is then

$$\%\eta = \frac{P_0(ac)}{P_i(dc)} \times 100\%$$

$$= \frac{{V_{CC}}^2 / 2R_L}{2{V_{CC}}^2 / \pi R_L} \times 100\%$$

$$= \frac{\pi}{4} \times 100\%$$

$$= 78.54\%$$

Efficiency in another form

✓ The maximum efficiency of a class B amplifier can also be expressed as follows:

$$P_0(ac) = \frac{{V_L}^2(p)}{2R_L}$$

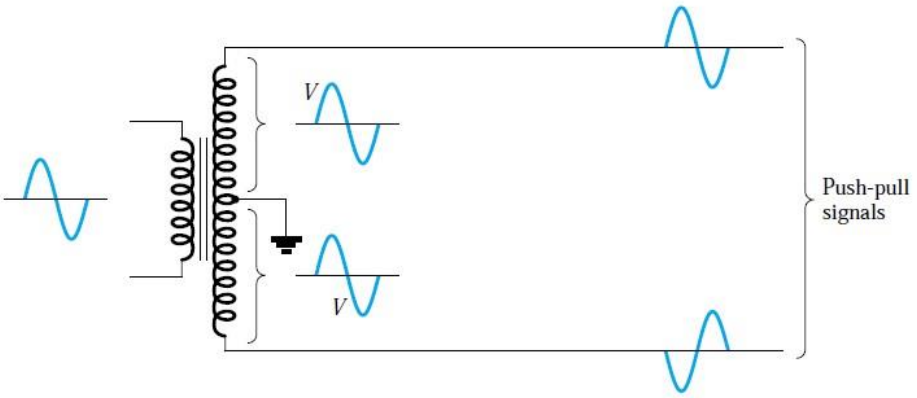
$$P_i(dc) = V_{CC} I_{dc} = V_{CC}[\frac{2}{\pi}\frac{V_L(p)}{R_L}]$$

$$\%\eta = \frac{\mathrm{P_0(ac)}}{\mathrm{P_i(dc)}} \times 100\% = \frac{{V_L}^2(p)/2R_L}{\mathrm{V_{CC}}[\frac{2}{\pi}\frac{V_L(p)}{R_L}]} \times 100\%$$

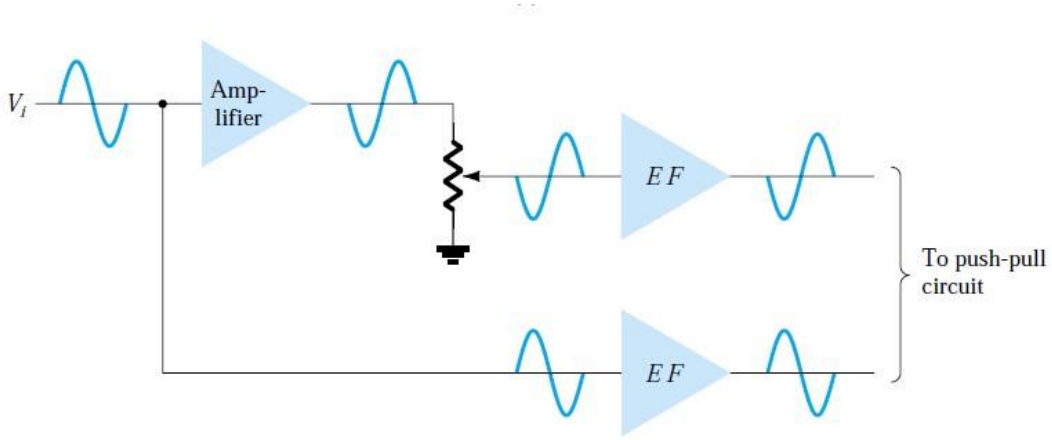
$$= 78.54\frac{V_L(p)}{V_{CC}} \times 100\%$$

Class B amplifier circuits

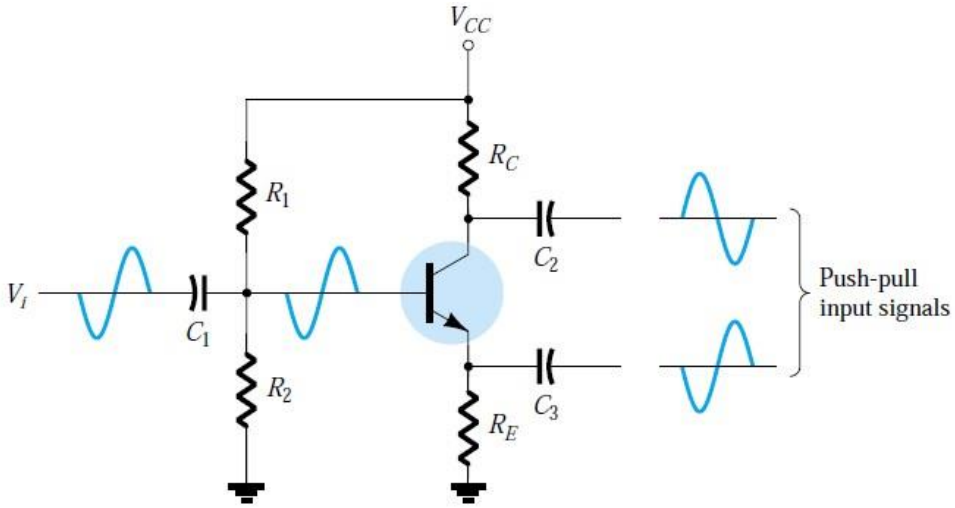
- ✓ A number of circuit arrangements for obtaining class B operation are possible.
- ✓ The input signals to the amplifier could be a single signal, the circuit then providing two different output stages, each operating for one-half the cycle.
- ✓ If the input is in the form of two opposite polarity signals, two similar stages could be used, each operating on the alternate cycle because of the input signal.
- ✓ One means of obtaining polarity or phase inversion is using a transformer, the transformer coupled amplifier having been very popular for a long time.
- ✓ Figure shows a center-tapped transformer to provide opposite phase signals.
- ✓ If the transformer is exactly center-tapped, the two signals are exactly opposite in phase and of the same magnitude.



- ✓ Opposite polarity inputs can easily be obtained using an op-amp having two opposite outputs or using a few op-amp stages to obtain two opposite polarity signals.



- ✓ The circuit of Fig. uses a BJT stage with in-phase output from the emitter and opposite phase output from the collector.



Transformer coupled push-pull amplifier

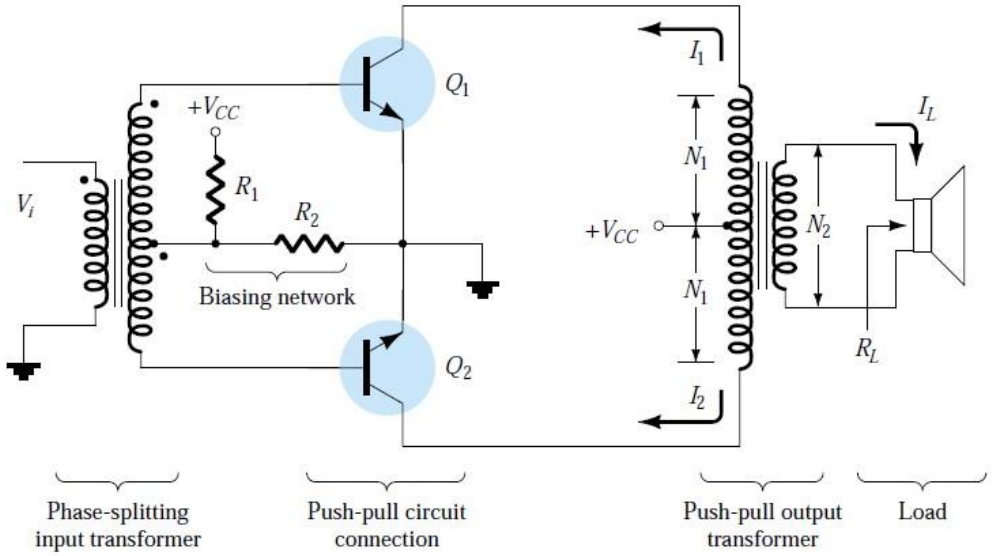
- ✓ The circuit of Fig. uses a center-tapped input transformer to produce opposite polarity signals to the two transistor inputs and an output transformer to drive the load in a push-pull mode of operation.

- ✓ During the first half-cycle of operation, transistor Q_1 is driven into conduction, whereas transistor $Q_2$is driven off.

- ✓ The current I_1through the transformer results in the first half-cycle of signal to the load.

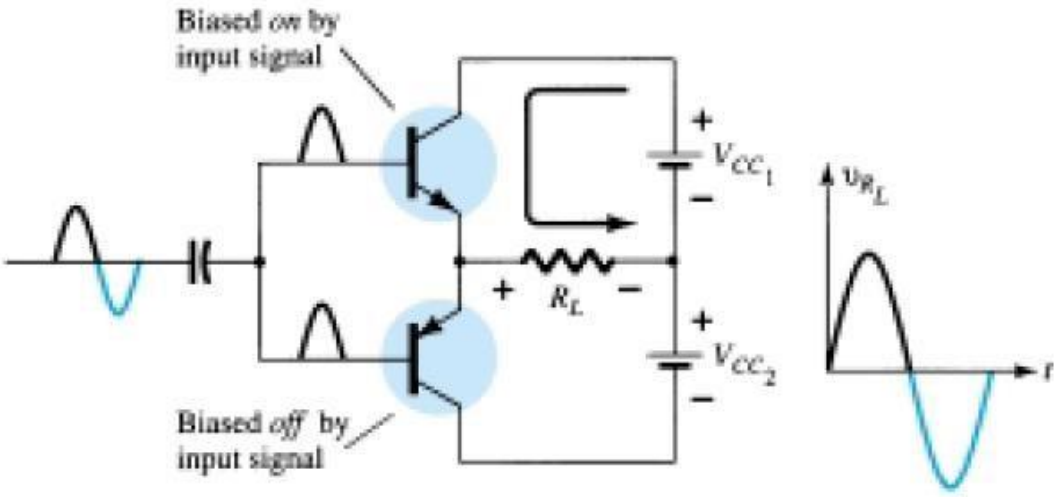
- ✓ During the second half-cycle of the input signal Q_2conducts whereas Q_1 stays off, the current I_2through the transformer resulting in the second half-cycle to the load.

- ✓ The overall signal developed across the load then varies over the full cycle of signal operation.



Complementary symmetry circuits

- ✓ Every transistor will conduct for half cycle.
- ✓ Single input signal is applied to the base of both transistors.
- ✓ npn transistor will be biased in conduction for positive half cycle of the input.
- ✓ During negative half cycle pnp transistor is biased into conduction when input goes to negative.



Disadvantages

- ✓ One disadvantage is that the need of two separate voltage supplies.
- ✓ Cross over distortion in the output signal.
- ✓ This cross over distortion is referred to as the nonlinearity in the output signal during cross over from positive to negative or vice-versa.

Amplifier distortion

- ✓ Any signal varying over less than the full 360^0 cycle is considered to have distortion.
- ✓ An ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version, the resulting waveform being a pure sinusoidal frequency sinusoidal signal.
- ✓ When distortion occurs, output will not be an exact duplicate of input signal (except for magnitude).
- ✓ Distortion can occur because the device characteristic is not linear. In this case non linear or amplitude distortion occurs.
- ✓ Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

- ✓ One technique for describing distorted but period waveforms uses Fourier analysis, a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples- these components are called ***harmonic components or harmonics.***

Harmonic Distortion

- ✓ A signal is considered to have harmonic distortion when there are harmonic frequency components.

- ✓ If fundamental frequency has amplitude A_1, and n^{th} frequency component has an amplitude of A_n.

- ✓ Harmonic distortion can be defined as

$$\%\, n^{th} harmonic\ distortion = \%D = \frac{|A_n|}{|A_1|} \times 100\%$$

Total harmonic distortion

When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based on the individual elements as combined by relation

$$\%\text{THD} = \sqrt{(\text{D}_2{}^2 + \text{D}_3{}^2 + \text{D}_4{}^2 + \cdots..)} \times 100\%$$

Second harmonic distortion

$$\text{D}_2 = \left| \frac{\frac{1}{2}((\text{I}_{\text{C}_{\max}} + \text{I}_{\text{C}_{\min}}) - \text{I}_{\text{C}_\text{Q}}}{(\text{I}_{\text{C}_{\max}} - \text{I}_{\text{C}_{\min}})} \right| \times 100\%$$

In voltage terms,

$$\text{D}_2 = \left| \frac{\frac{1}{2}(\text{V}_{\text{CE}_{\max}} + \text{V}_{\text{CE}_{\min}}) - \text{V}_{\text{CE}_\text{Q}}}{(\text{V}_{\text{CE}_{\max}} - \text{V}_{\text{CE}_{\min}})} \right| \times 100\%$$

Power of signal having distortion

- ✓ Power delivered to the load resistor $R_C$due to the fundamental component of the distorted signal is

$$P_1 = \frac{{I_1}^2 R_C}{2}$$

- ✓ Total power due to all the harmonic components of the distorted signal is,

$$P = ({I_1}^2 + {I_2}^2 + {I_3}^2 + \cdots)\frac{R_C}{2}$$

- ✓ In terms of Total harmonic distortion

$$P = (1 + {D_2}^2 + {D_3}^2 + \cdots){I_1}^2\frac{R_C}{2}$$

$$\boxed{P = (1 + THD^2)P_1}$$